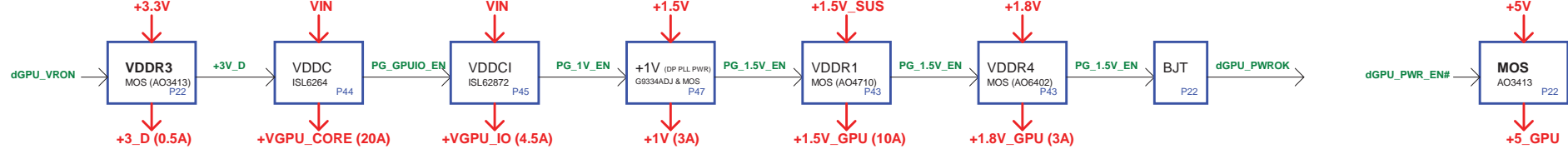
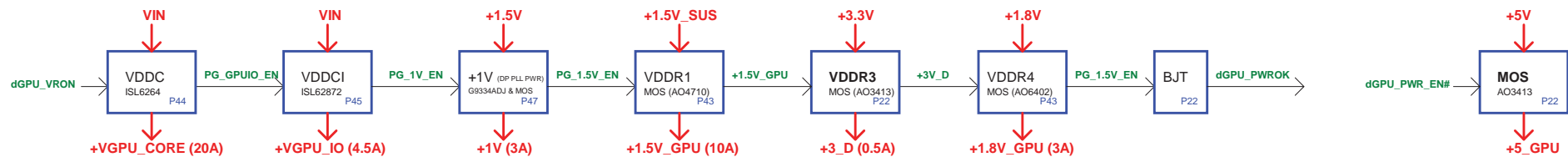


GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



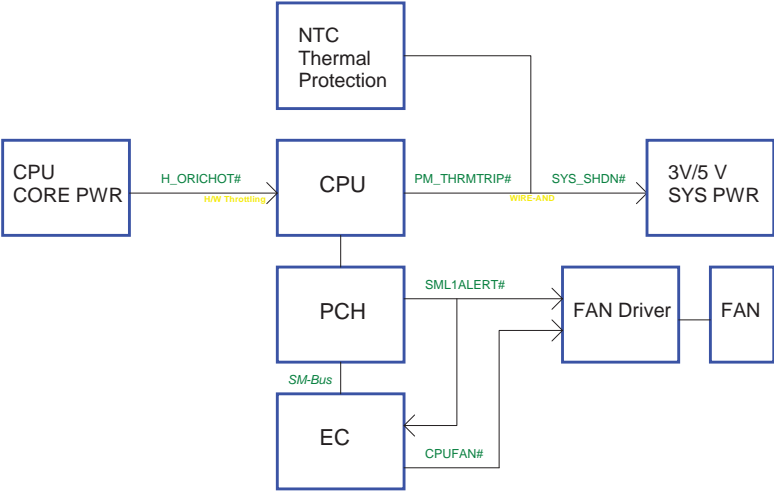
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)

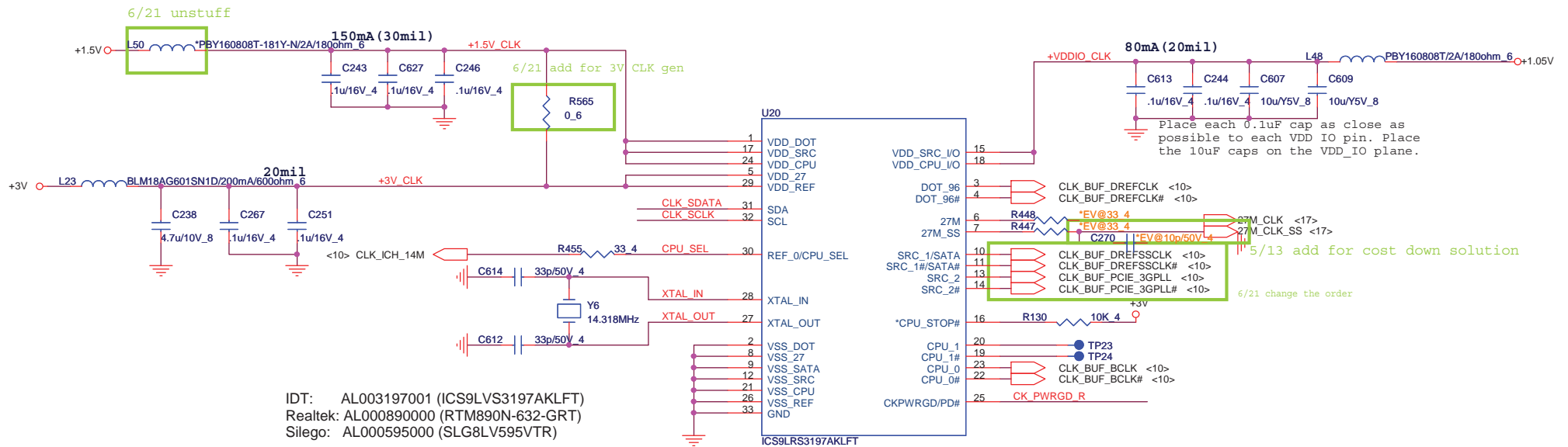


Power States

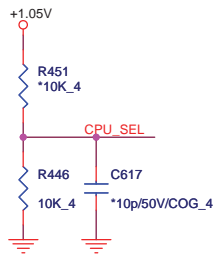
POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



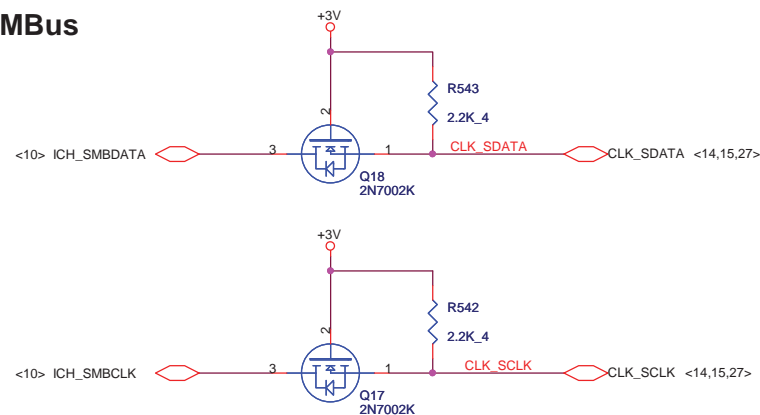


CPU_CLK select

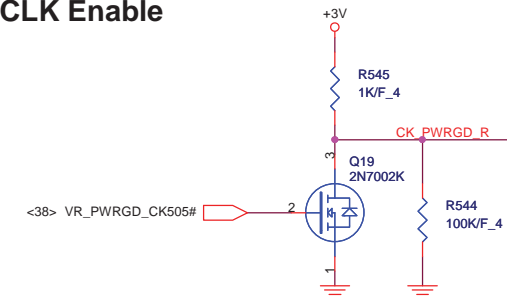


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus

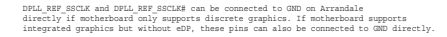


CLK Enable



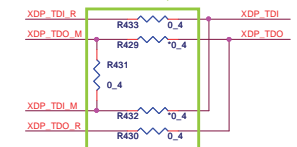
Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	Clock Generator	1A
Date:	Tuesday, June 22, 2010	Sheet 3 of 45



Layout Note: Place these resistors near Processor

Thermaltrip protect



Scan Chain (Default)	STUFF -> R469, R491, R507 NO STUFF -> R489, R490
CPU Only	STUFF -> R490, R491 NO STUFF -> R469, R489, R507
GMCH Only	STUFF -> R489, R507 NO STUFF -> R491, R490, R469



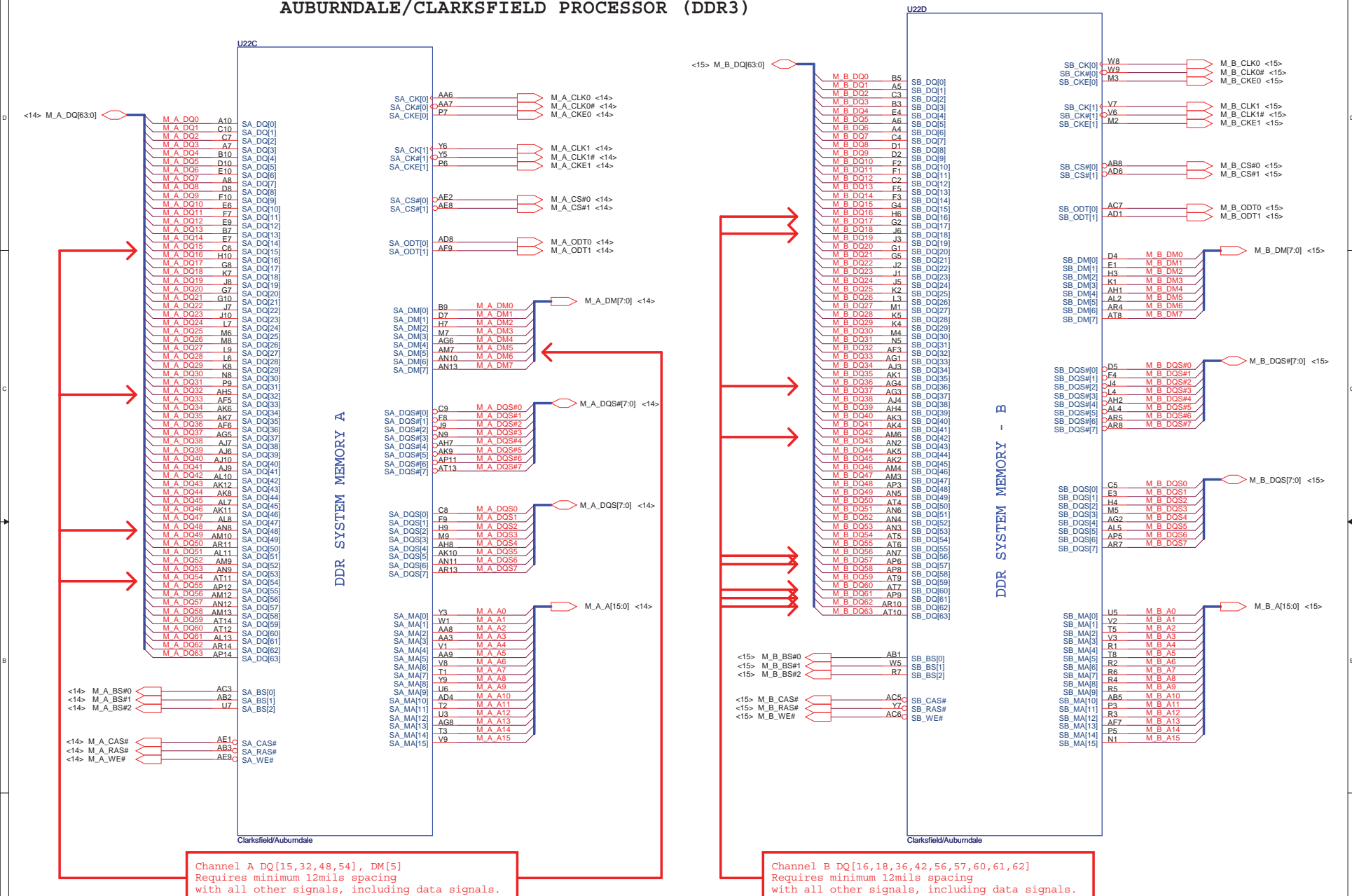
Quanta Computer Inc.

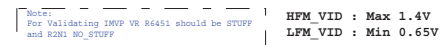
PROJECT : ZQ9

Size	Document Number	Rev
	AUBURND 1/4	1A
Date:	Tuesday, June 22, 2010	Sheet 4 of 45

Date: Tuesday, June 22, 2010 Sheet 4 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

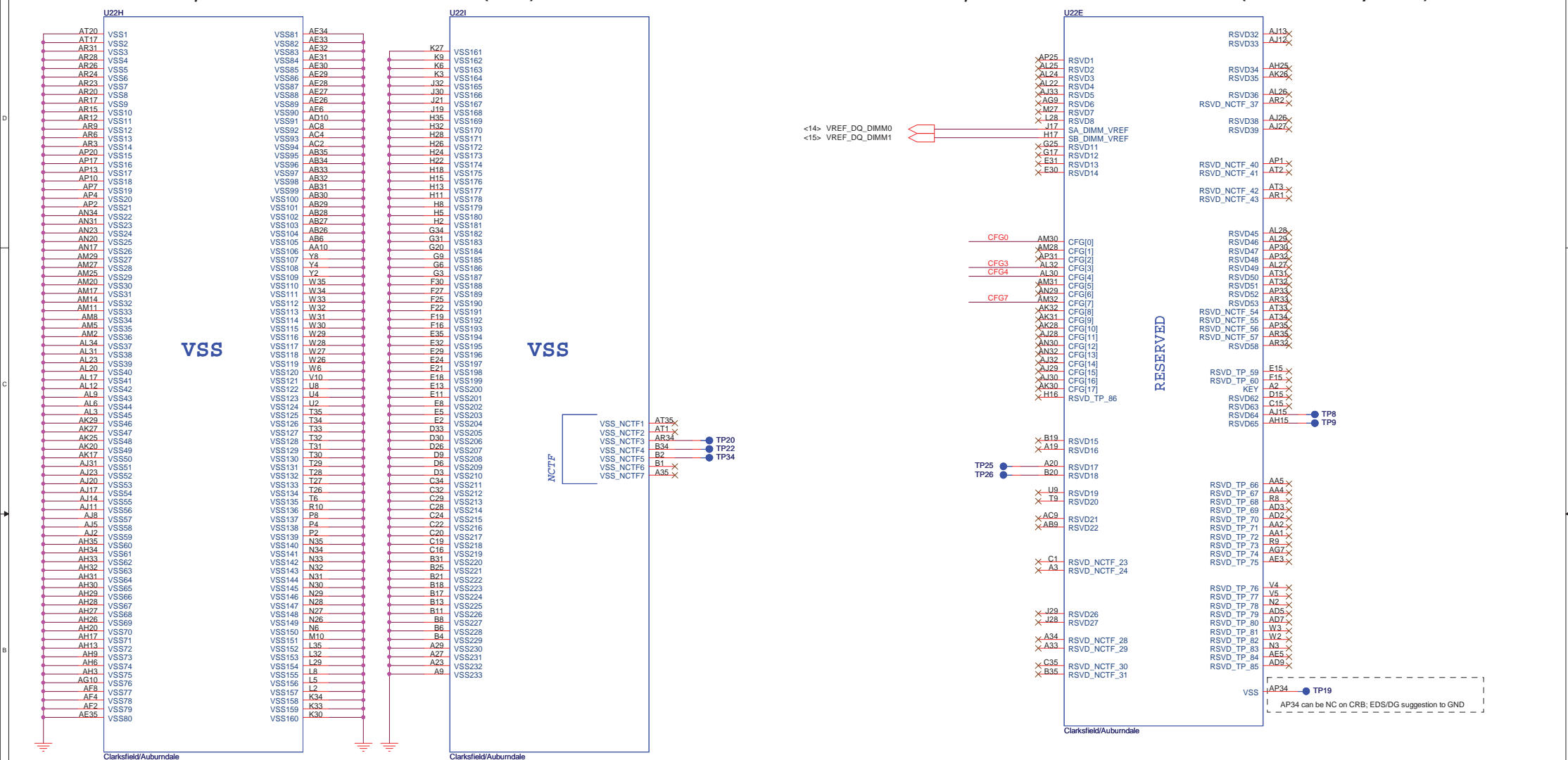




Size	Document Number AUBURND 3/4 (PWR)	Rev 1A
Date:	Tuesday, June 22, 2010	Sheet 6 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)



Processor Strapping

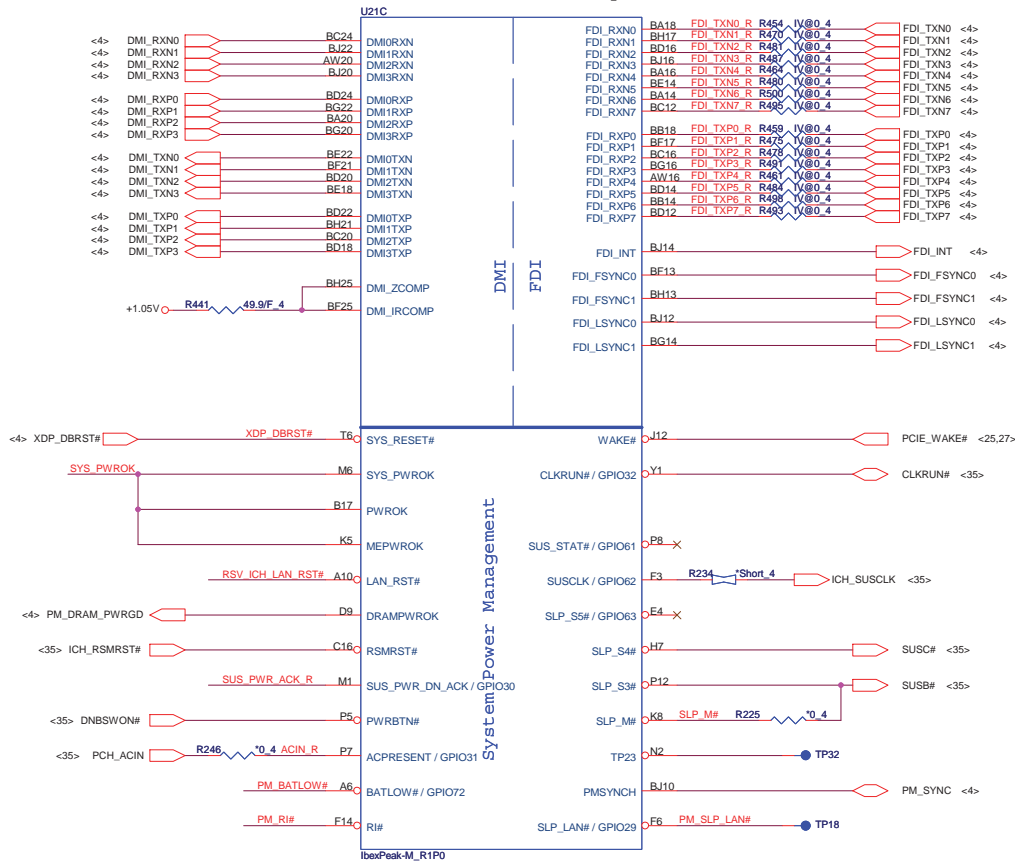
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 ~3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 ~3.01K_F_4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 ~3.01K
T h b e t p				CFG7 R126 ~3.01K_F_4

IBEX PEAK-M (DMI, FDI, GPIO)

AC-coupling CAP place close to PCH

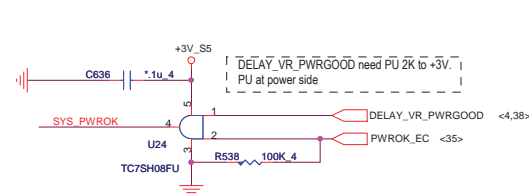
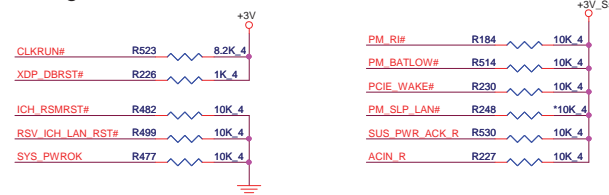
0-ohm resistor place close to PCH

IBEX PEAK-M (LVDS, DDI)



PCH Pull-high/low

System PWR_OK



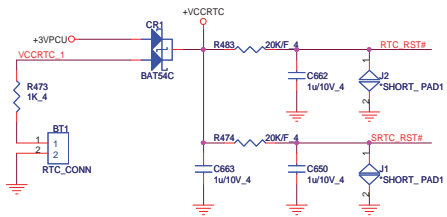
Quanta Computer Inc.

PROJECT : ZQ9

Size Document Number
IBEX PEAK-M 1/6

Date: Tuesday, June 22, 2010 Sheet 8 of 45 Rev 1A

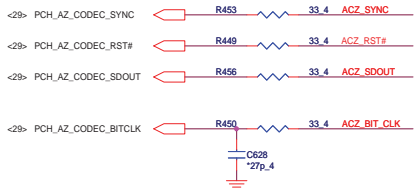
RTC Circuitry



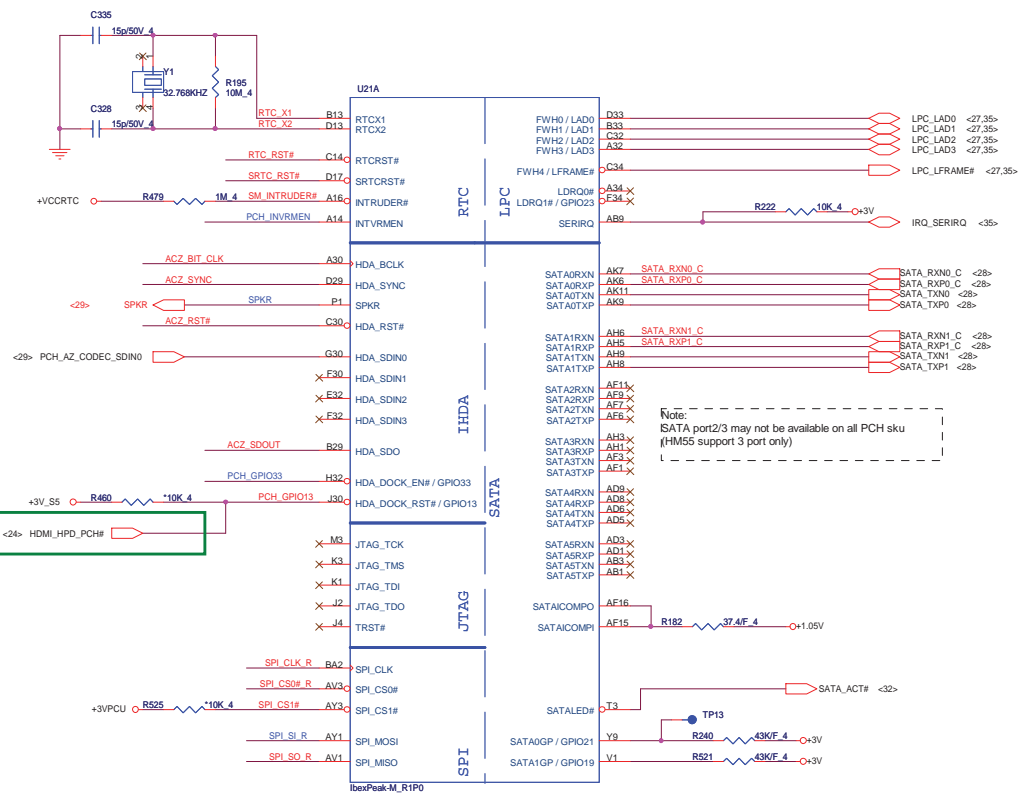
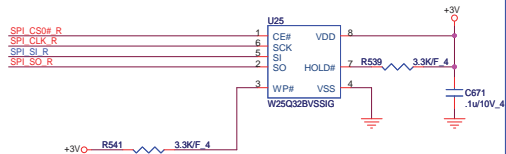
HDA_SYNC (PCH strap pin)

Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V

HDA Bus

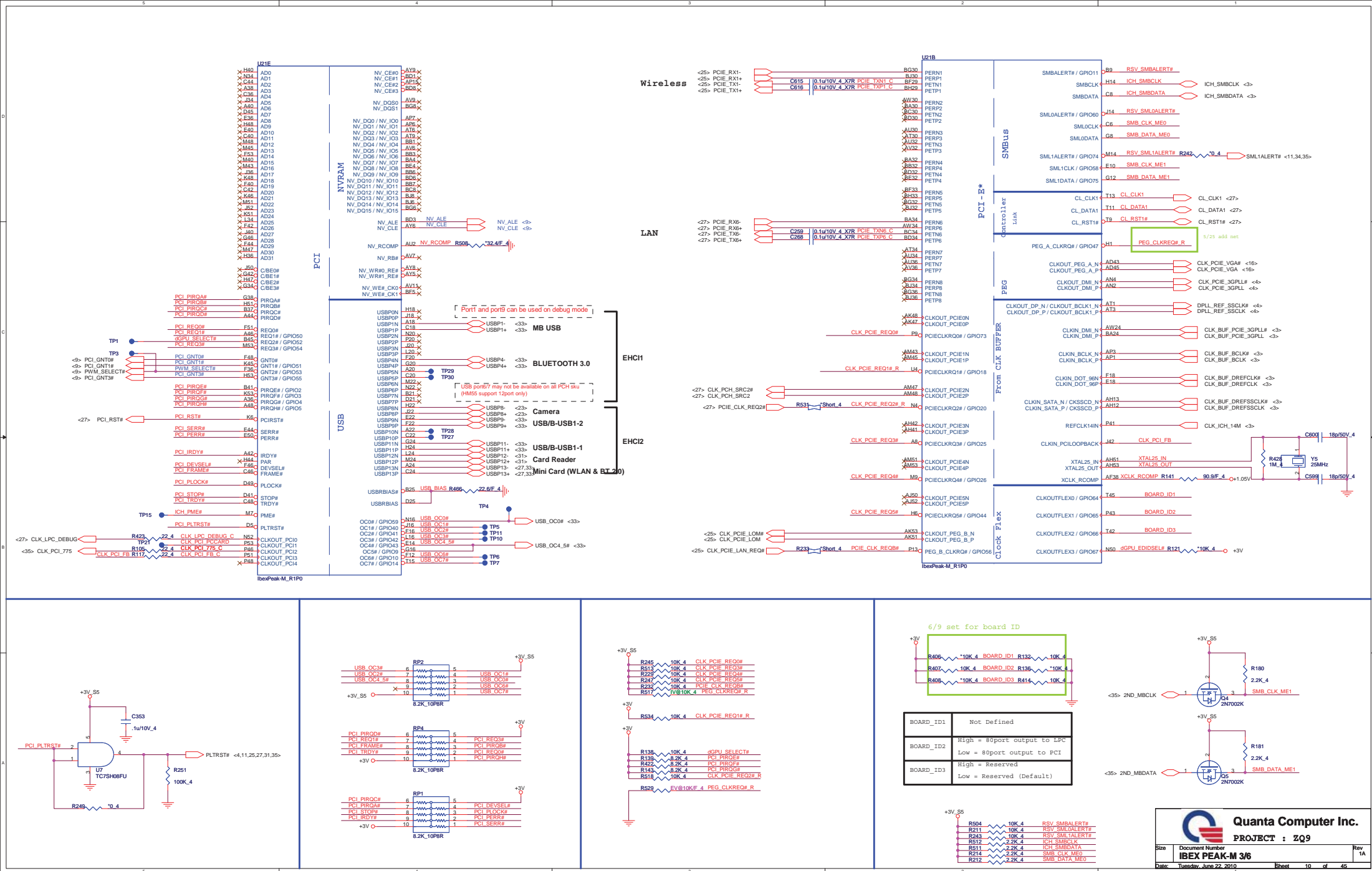


PCH SPI



PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K 6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 1K 4 SPKR
HDA_DOCK#EN /GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R184 1K 4 R146 1K 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K 4 R122 1K 4 R131 1K 4
GNT2# /GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	PWM_SELECT# R158 1K 4
GNT3# /GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	PCI_GNT3# R421 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	NV_ALE R202 1K 4
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	NV_CLE R206 1K 4
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	SV_GPIO8 R204 10K 4 R203 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R244 1K 4
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	PCH_GPIO27 R221 10K 4

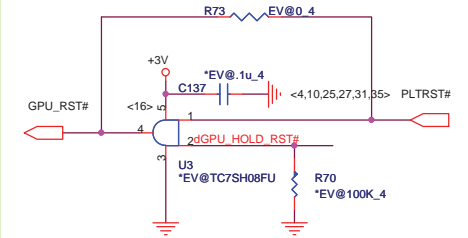


IBEX PEAK-M (GPIO, VSS_NCTF, RSVD)

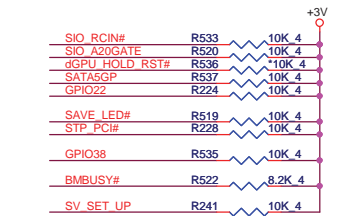
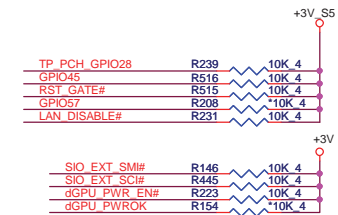


GPU RST#

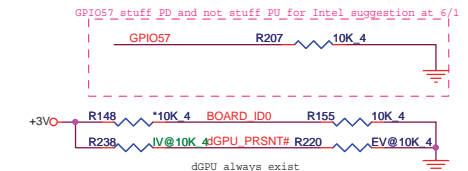
5/18 change for discrete only



GPIO Pull-up/Pull-down



SV_SET_UP 1-X High = Strong (Default)



dGPU always exist

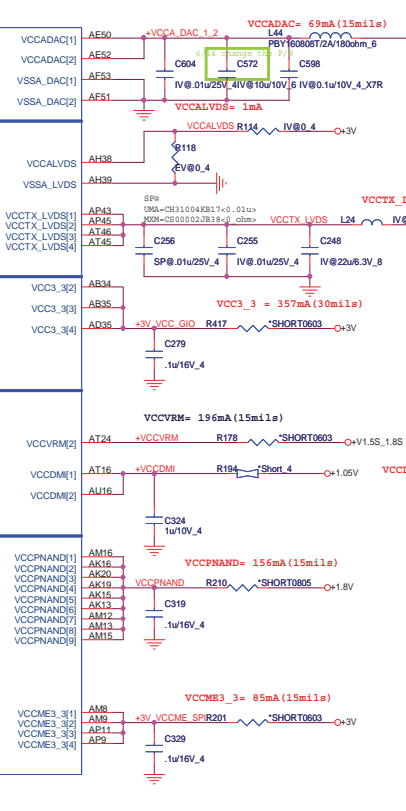
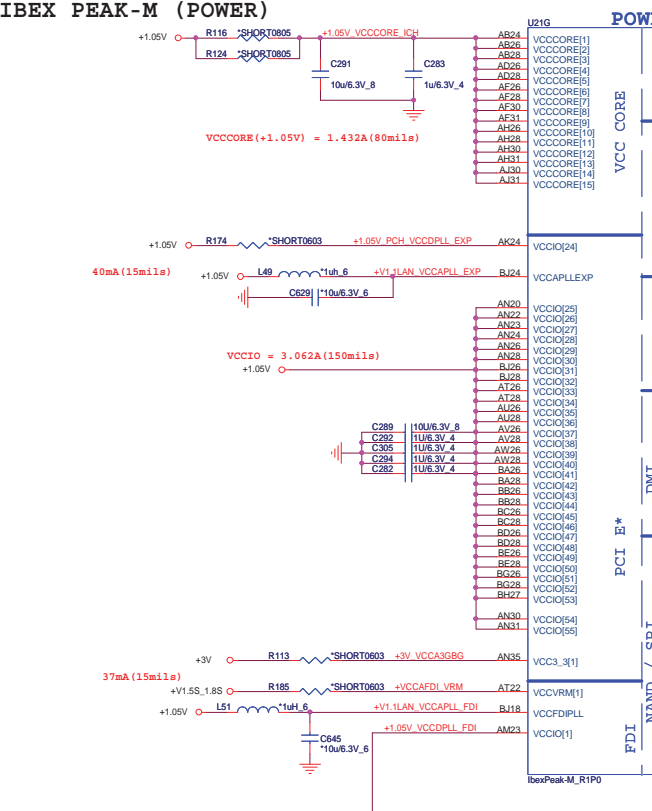
5/18 separate for 14" & 15"

BOARD_ID0	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable

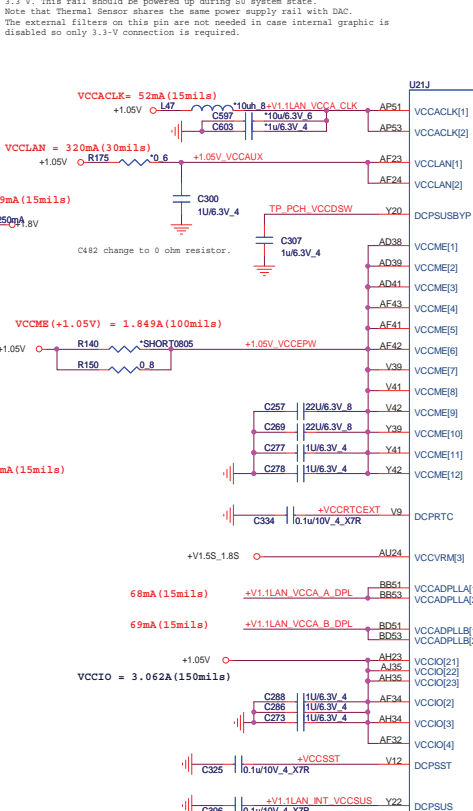


Quanta Computer Inc.
PROJECT : ZQ9

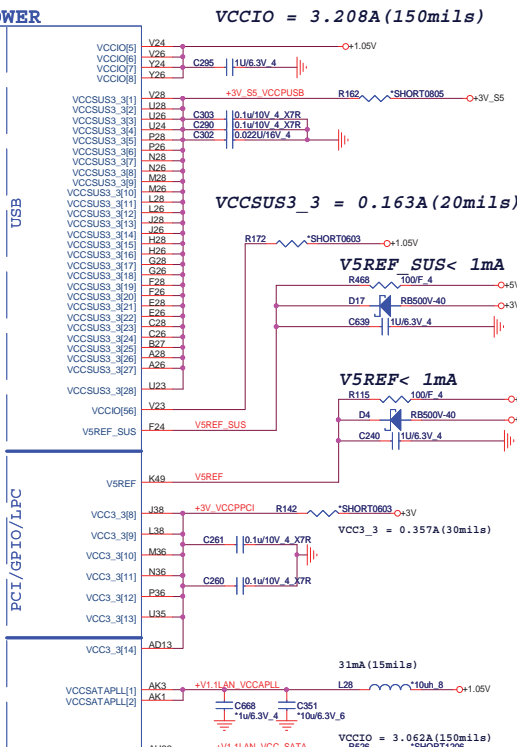
IBEX PEAK-M (POWER)



Note that Thermal Sensor shares the same power supply rail with DAC. The external filters on this pin are not needed in case internal graphs disabled so only 3.3-V connection is required.

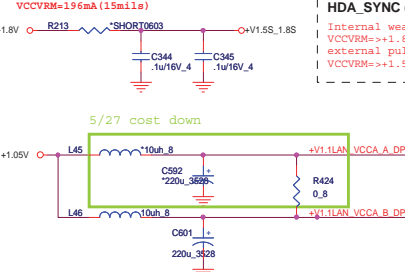


POWE

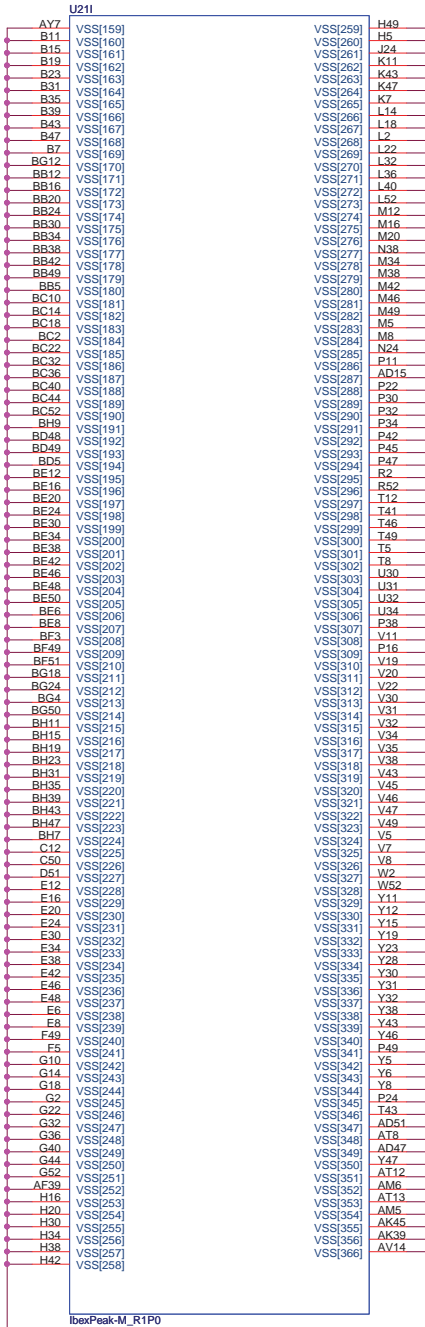
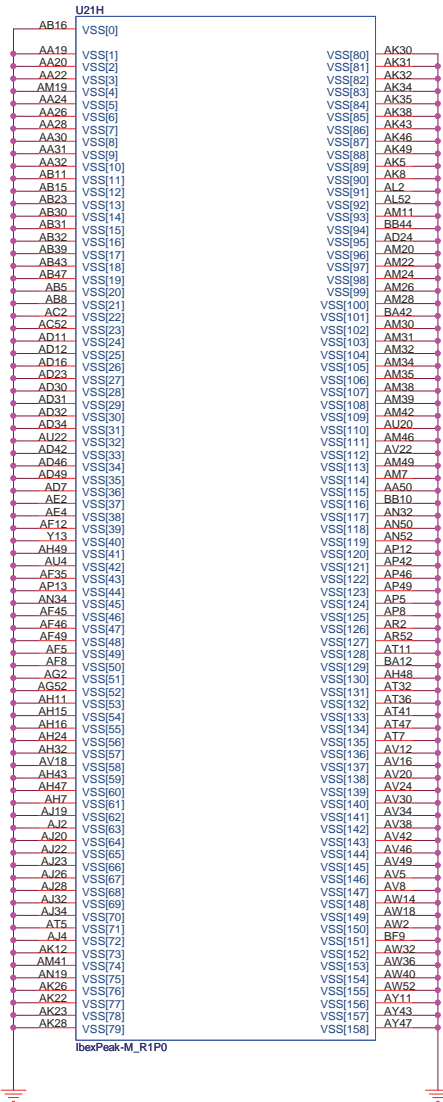


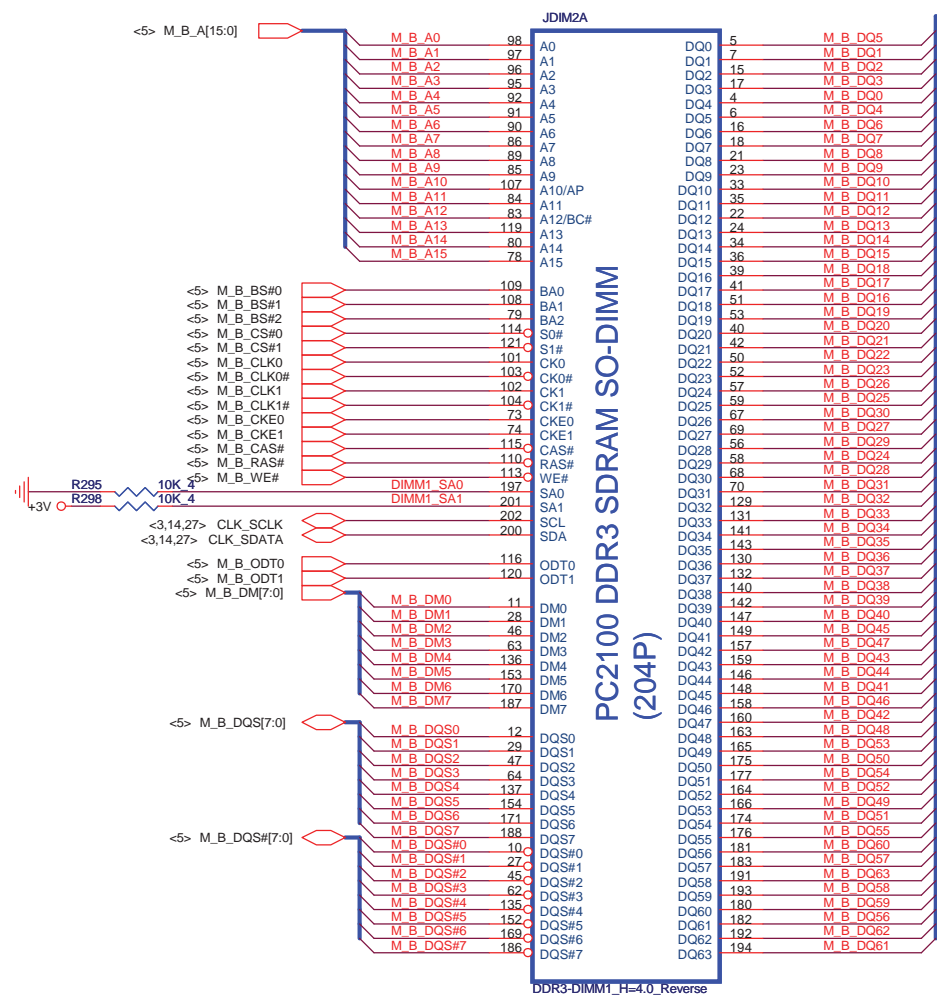
```
VRM enable by strap pin GPIO27
which supply clean 1.05V for
[VCCACLK,VCCAPLLEXP,VCCFDIPLL,VCCSATAPLL]
```

```
HDA_SYNC (PCH strap pin)
Internal weak pull-down
VCCVRM=>+1.8V (default)
external pull-up
VCCVRM=>+1.5V
```

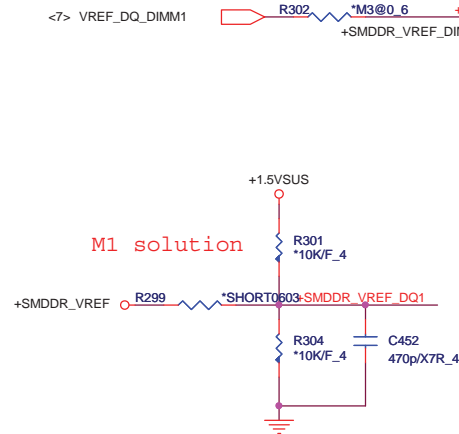


IBEX PEAK-M (GND)



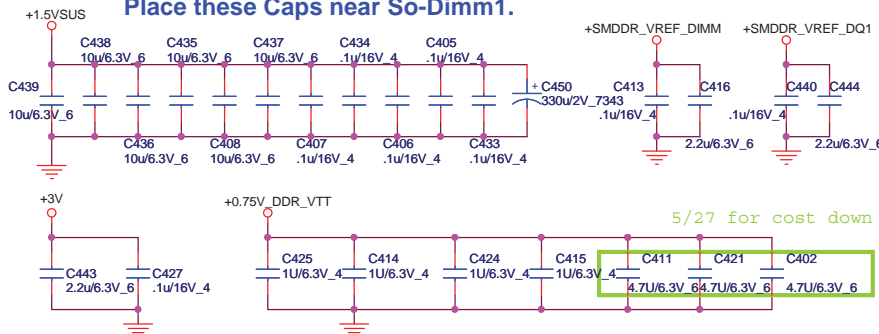


M3 solution



M1 solution

Place these Caps near So-Dimm1.



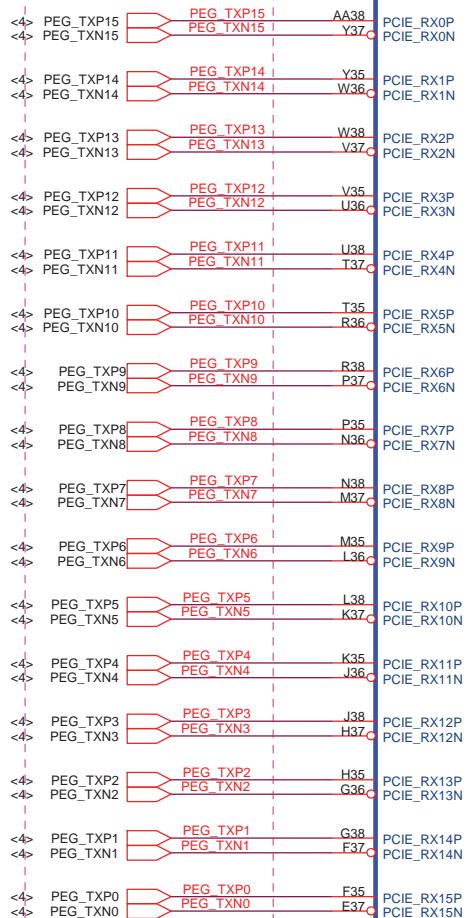
Quanta Computer Inc.

PROJECT : ZQ9

GPU_1(VGA)

<4> PEG_TXP[0..15] PEG_TXN[0..15]
 <4> PEG_RXP[0..15] PEG_RXN[0..15]

0518 SWAP PCIE for VGA side



<10> CLK_PCIE_VGA
 <10> CLK_PCIE_VGA#

For Broadway, Madison and Park the PWRGOOD ball must be connected to ground



<11> GPU_RST#

U15A

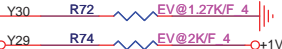
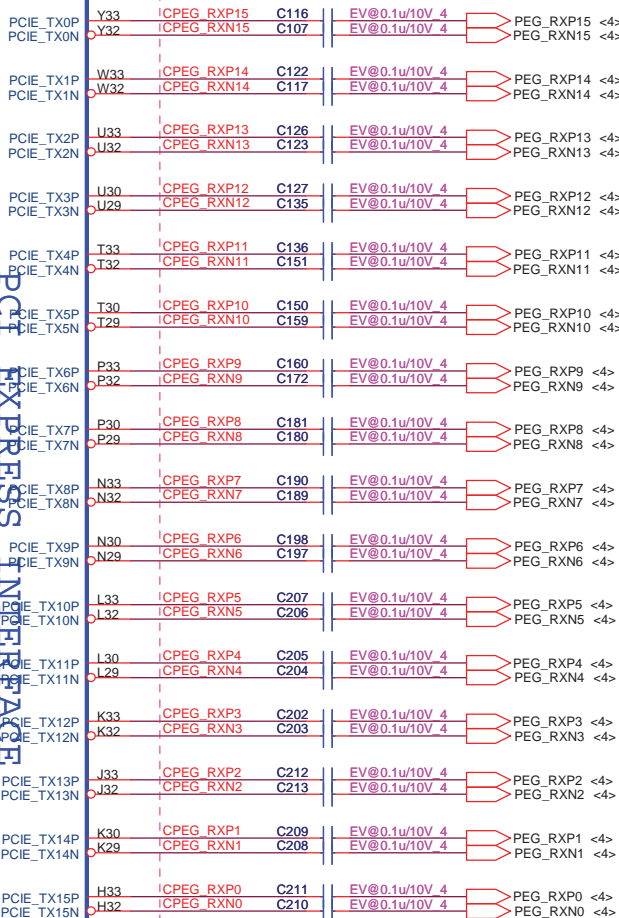
CLOCK
 PCIE_REFCLKP
 PCIE_REFCLKN

CALIBRATION
 PCIE_CALRP
 PCIE_CALRN

EV@Park_M2

0518 SWAP PCIE for VGA side

PCI EXPRESS INTERFACE



+1.0V

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison	AJ007720T02
Park	AJ077400T08



Quanta Computer Inc.
 PROJECT : ZQ9

Size	Document Number	Rev
	Madison/Park M2-PCIE I/F	1A

Date: Tuesday, June 22, 2010 Sheet 16 of 45

GPU_2(VGA)

GPU Power-on sequence

- 1 => MAINON
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => GPU_RST#

1.8V GPIO

NC on Park

NC on Park

Channel D N.C for Park-M2

EV@Park_M2

DAC2 will be NC on future ASIC

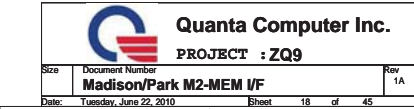
HDMI

DDC AUX4 NC for Park M2

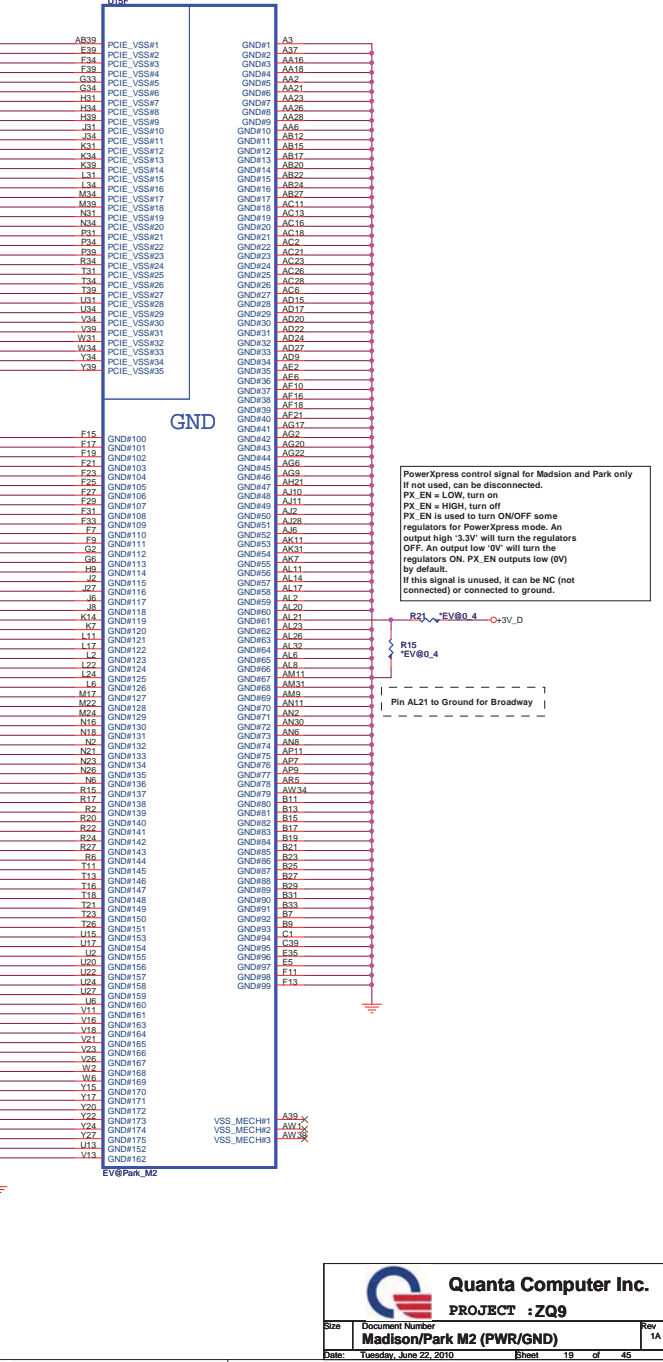
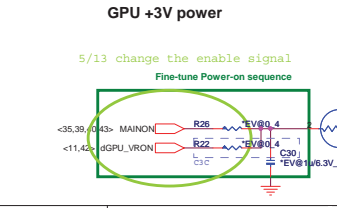
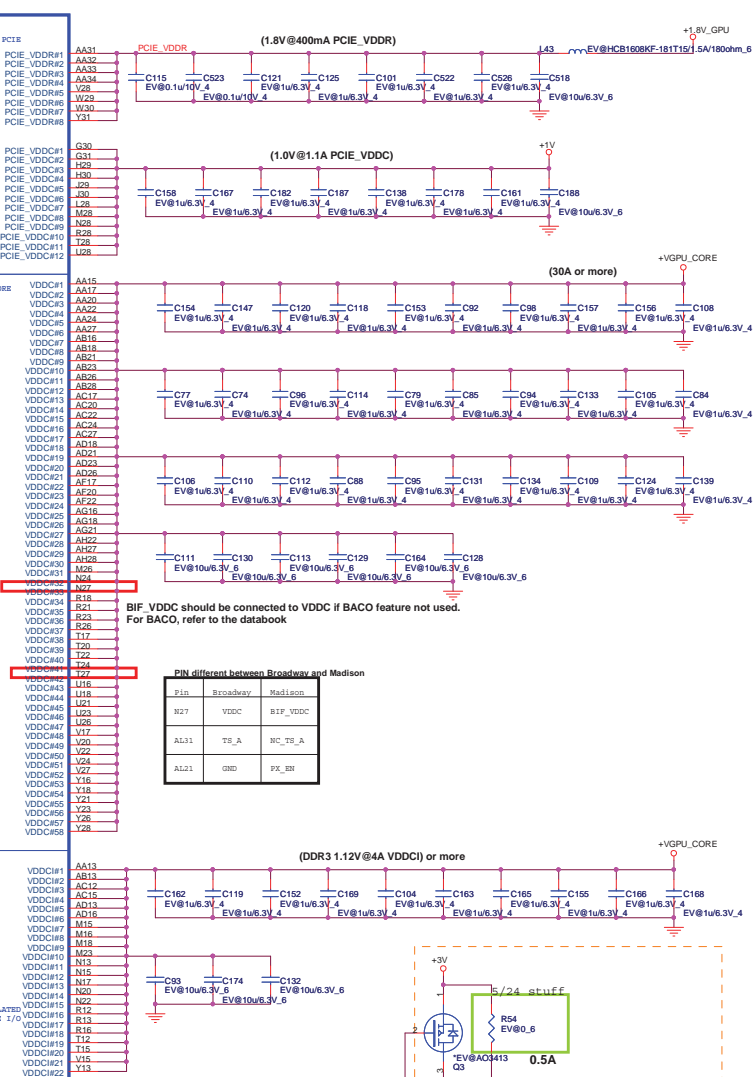
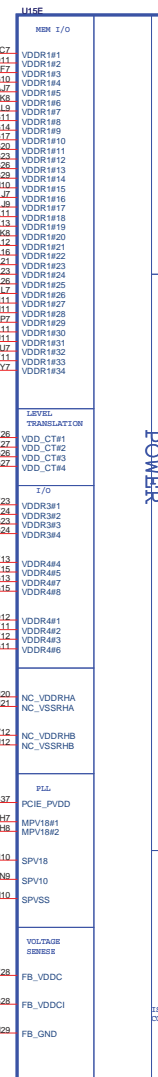
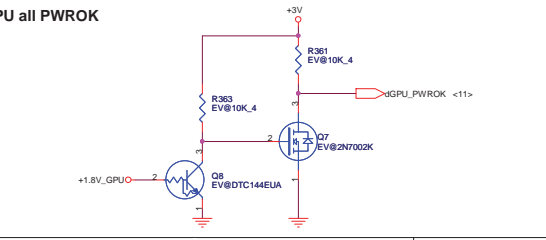
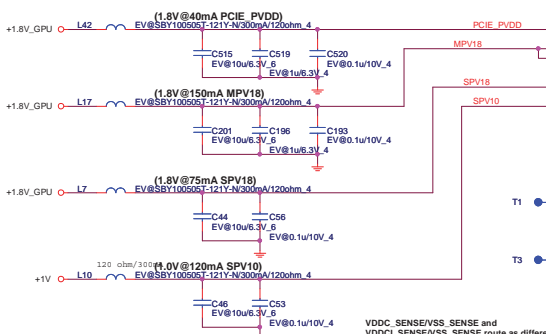
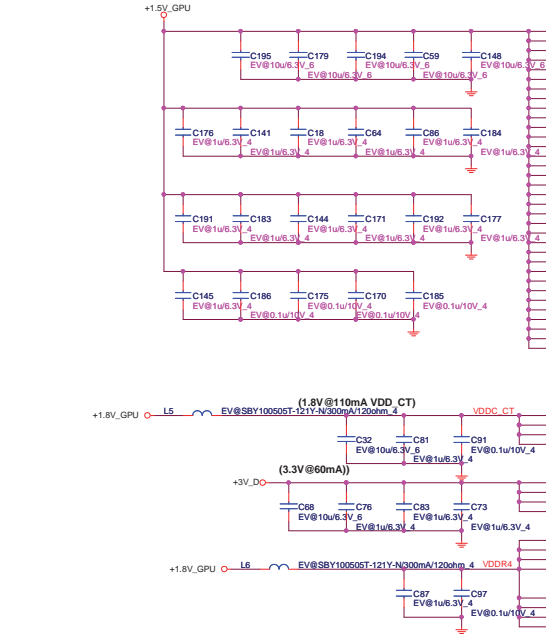
LVDS

CRT

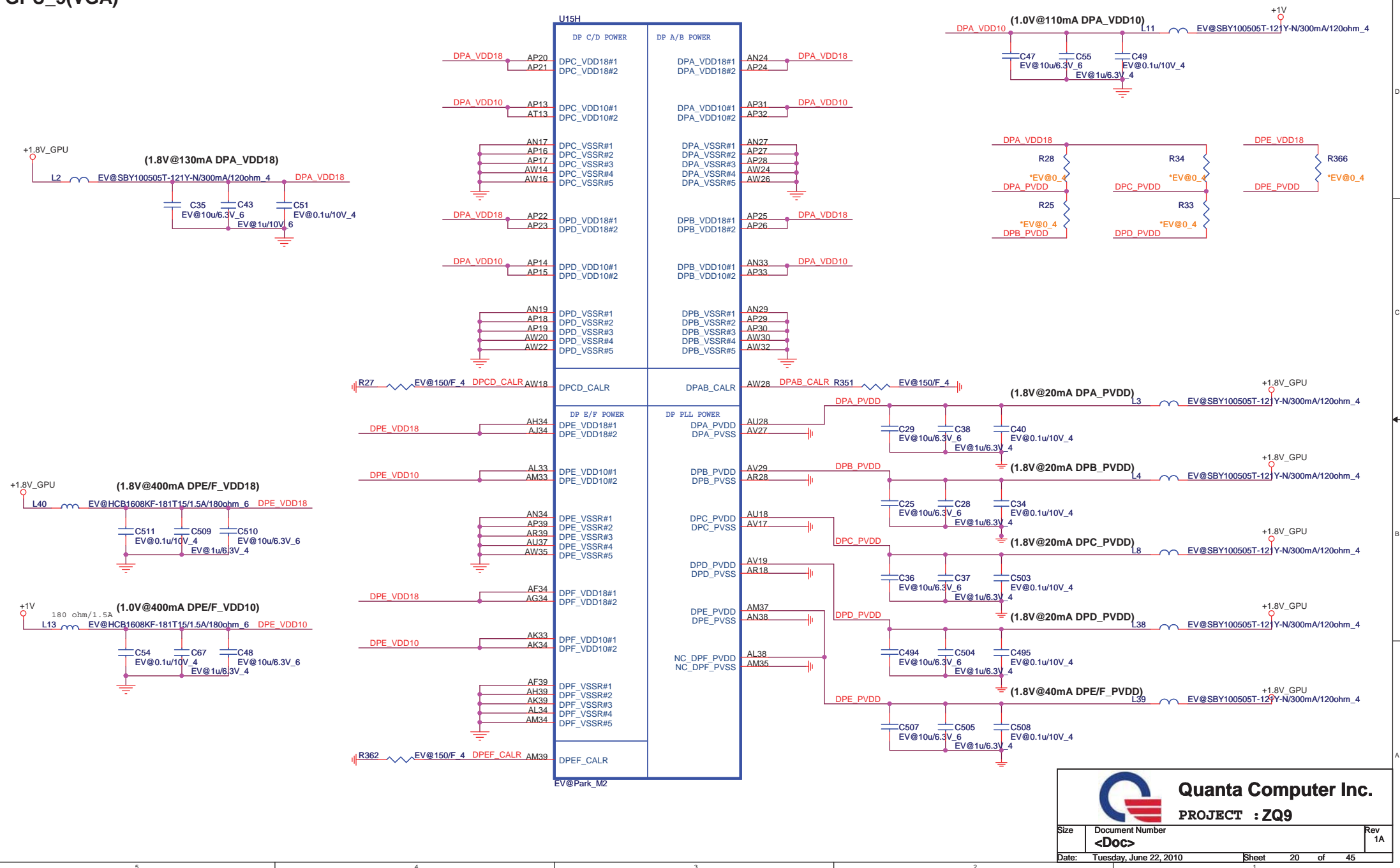
DDC AUX7 NC for Park M2



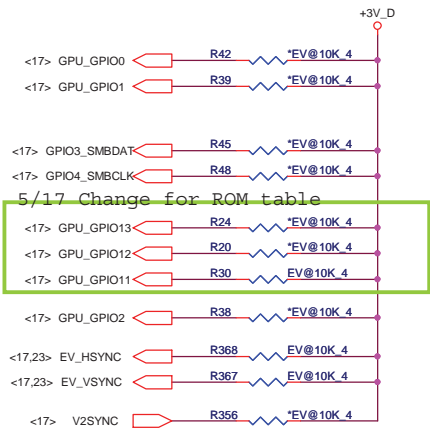
GPU_4(VGA)



GPU_5(VGA)



PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIe DEVICE AS 2.5GT/S CAPABLE 1 = PCIe DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

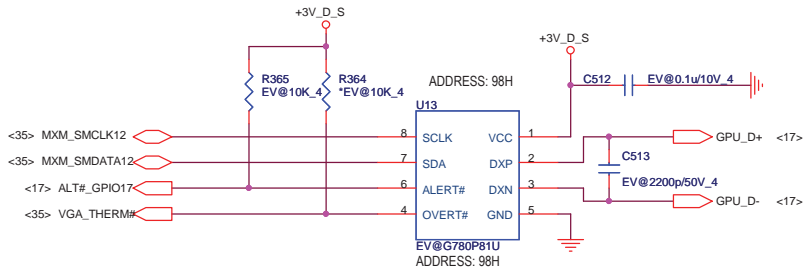
EEPROM(VGA) 5/17 delete EEPROM

DDR3 Memory Aperture size(GPU)

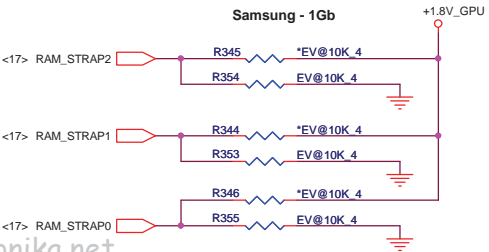
Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000


USD0.16



DDR3 Memory size					
Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD					
	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.



Quanta Computer Inc.
PROJECT : ZQ9

Size

Document Number

Strip/Thermal

Date: Tuesday, June 22, 2010

Sheet 21 of 45

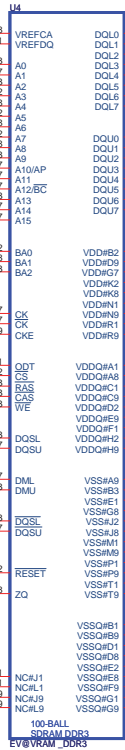
Rev 1A

CHANNEL B: 512MB DDR3 (16*64M*4pcs)

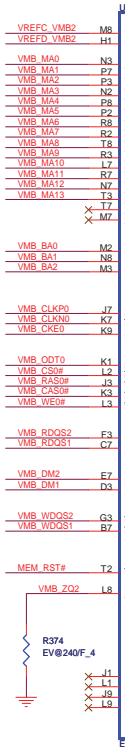
Park, M92M Use Channel B Memory Interface Only

<18> VMB_DQ[63..0]
<18> VMB_DM[7..0]
<18> VMB_RDOQS[7..0]
<18> VMB_WDQS[7..0]

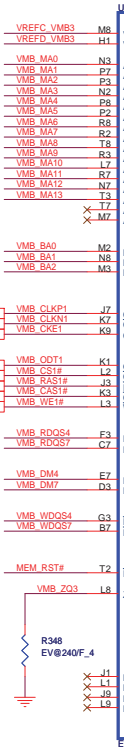
QSA[7..0]
QSA# [7..0]



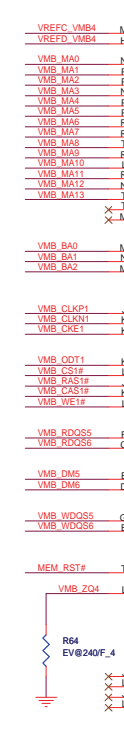
BOT Down



TOP Down

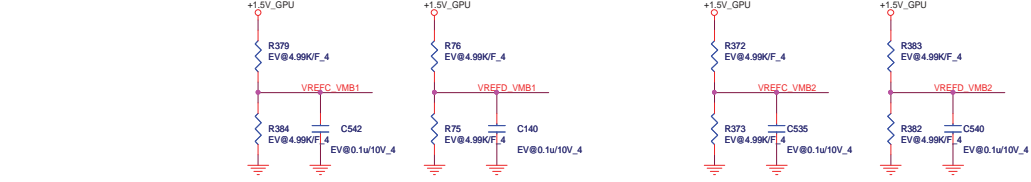


TOP Up

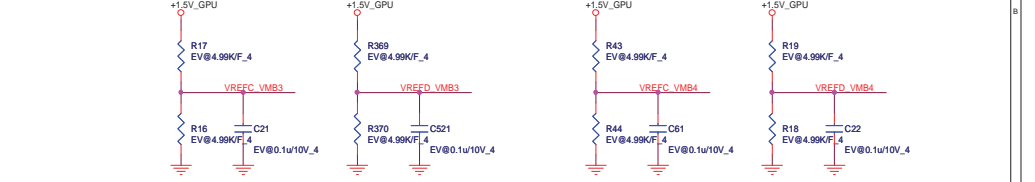


BOT Up

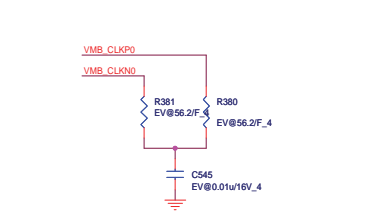
Group-B0 VREF



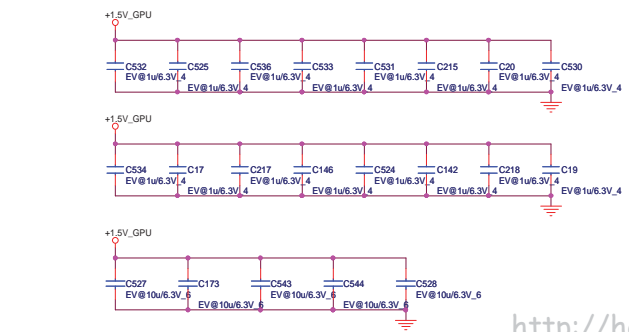
Group-B1 VREF



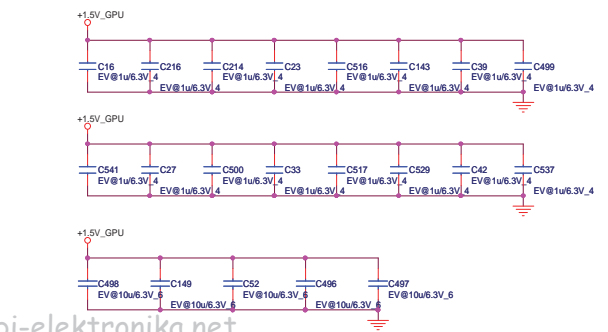
MEM_B0 CLK



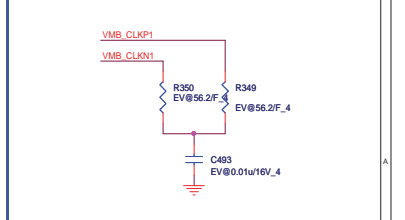
Group-B0 decoupling CAP



Group-B1 decoupling CAP



MEM_B1 CLK

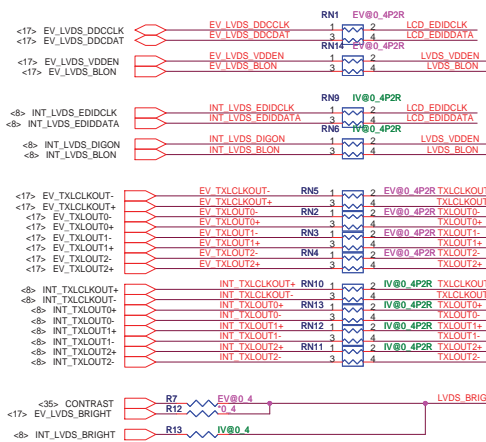


CV @

<> INT_CRT_RED	INT CRT RED	R95	IV@0.4	VGA_RED
<> INT_CRT_GRN	INT CRT GRN	R94	IV@0.4	VGA_GRN
<> INT_CRT_BLU	INT CRT BLU	R93	IV@0.4	VGA_BLU
<> INT_VSYNC	INT VSYNC	Rn7	IV@0.4P2R	VSYNC
<> INT_HSYNC	INT HSYNC	3	4	HSYNC
<> INT_CRT_DDCDAT	INT CRT DDCDAT	Rn8	IV@0.4P2R	CRTDDATA
<> INT_CRT_DDCCLK	INT CRT DDCCLK	1	4	CRTDCLK
<17> EV_CRT_BLU	EV CRT BLU	R391	EV@0.4	VGA_BLU
<17> EV_CRT_GRN	EV CRT GRN	R397	EV@0.4	VGA_GRN
<17> EV_CRT_RED	EV CRT RED	R395	EV@0.4	VGA_RED
<17.21> EV_VSYNC	EV VSYNC	Rn9	EV@0.4P2R	VSYNC
<17.21> EV_HSYNC	EV HSYNC	1	4	HSYNC
<17> EV_CRTCLK	EV CRTCLK	Rn16	EV@0.4P2R	CRTDCLK
<17> EV_CRTDATA	EV CRTDATA	1	4	CRTDDATA

The schematic diagram illustrates the VGA output circuit for the CM2009-Q20R. The top portion shows the external components, including the 2x3 pin header for VGA signals (RED, GRN, BLU) and the 15-pin D-sub connector (CN8). The signals are routed through a series of resistors (R189, R177, R165) and capacitors (C322, C308, C293, C637, C647, C653) to the connector. The bottom portion shows the internal circuitry of the CM2009-Q20R, featuring the U23 chip. The chip's inputs (VGA_SYNC, VCC_DDC, VCC_VIDEO, VIDEO_1, VIDEO_2, VIDEO_3, GND) are connected to the external signals. The chip's outputs (CRT_VSYNC2, CRT_HSYNC2, CRT_R1, CRT_G1, CRT_B1, DDC_IN1, DDC_IN2, DDC_OUT1, DDC_OUT2) are connected to the 15-pin connector. A note indicates a change from 6/21 to 0 ohm for the CRT_VSYNC2 and CRT_HSYNC2 signals. The circuit also includes various capacitors (C301, C331, C315) and resistors (R458, R457, R462, R469, R452, R476) for signal conditioning and timing.

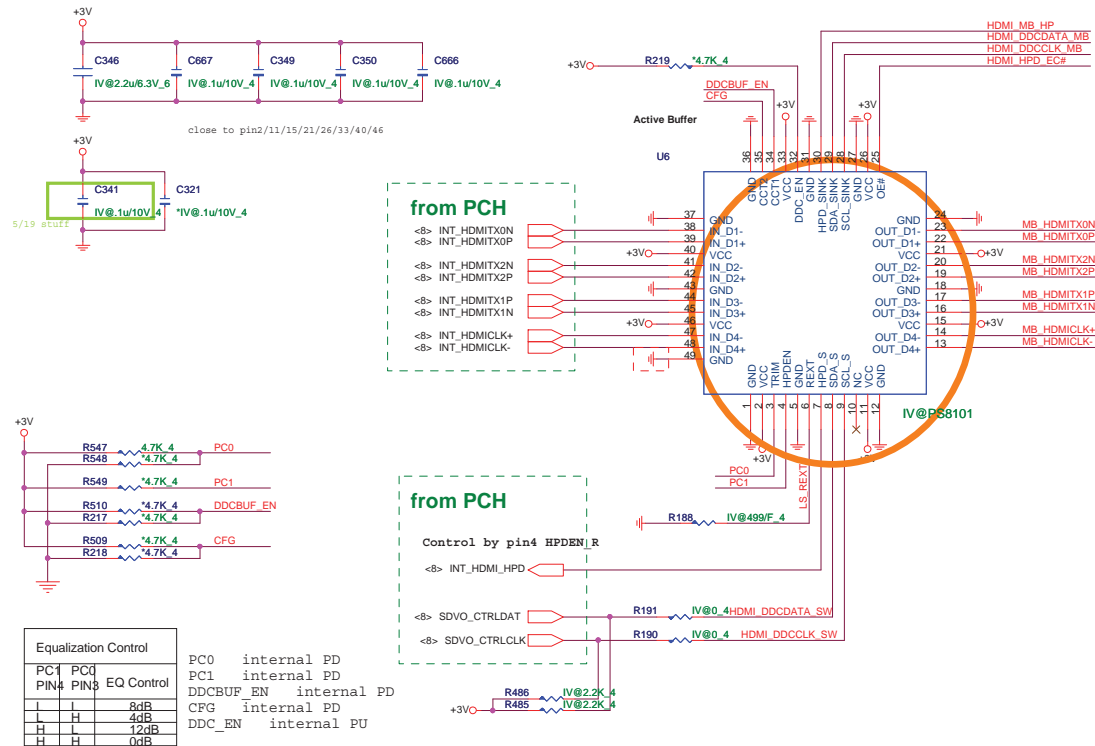
0_ohm Resistor place close to Joint-Point



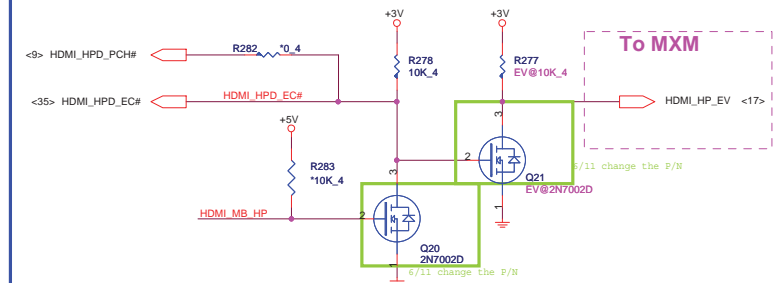
The schematic diagram illustrates the BLON driver circuit. It features a +3V supply connected to a network of resistors and transistors. Resistor R377 (10K_4) is connected to the +3V supply and the base of transistor Q10 (2N7002K). Resistor R376 (10K_4) is connected to the collector of Q10 and the base of transistor Q9 (DTC144EUA). Resistor R378 (100K_4) is connected to the emitter of Q10 and ground. Resistor R375 (100K_4) is connected to the +3V supply and the collector of Q9. Transistor Q9 is also connected to a diode D14 (BAS316) and the output BL_ON. A note indicates 'LID591#, EC internal PU' and 'EC_FPBACK# <35>'.

I@ HDMI LEVEL SHIFTER

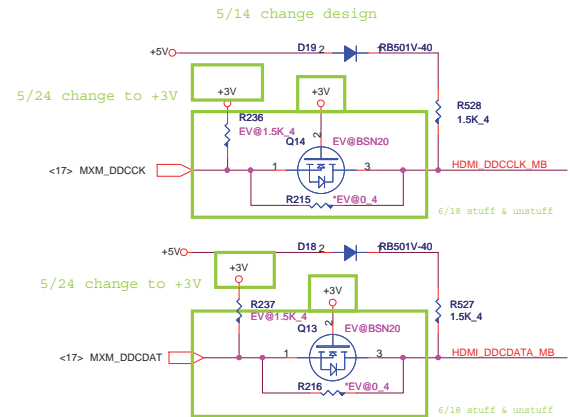
IV@
EV@



SW@HDMI-detect



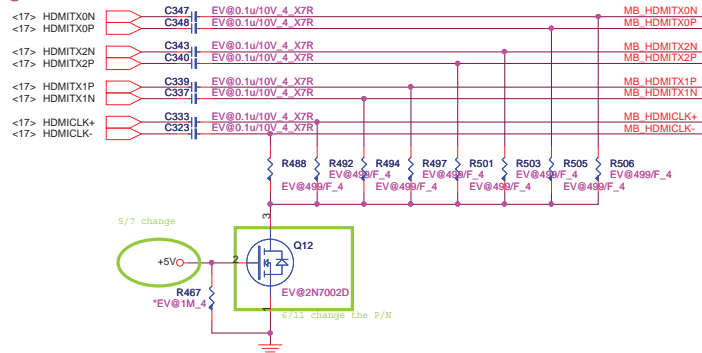
I2C



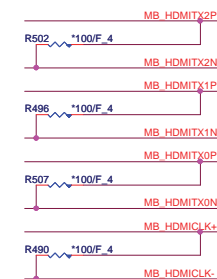
AC-coupling CAP place close to HDMI-connector

Switchable Graphic HDMI source

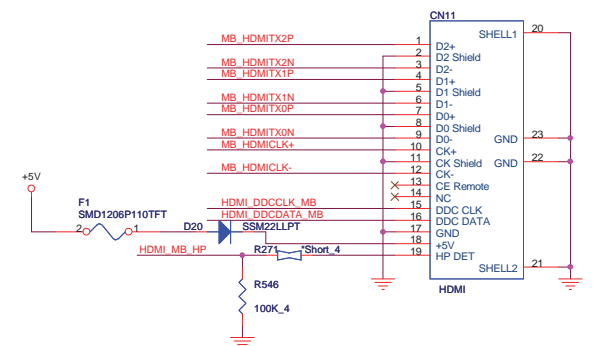
From GPU



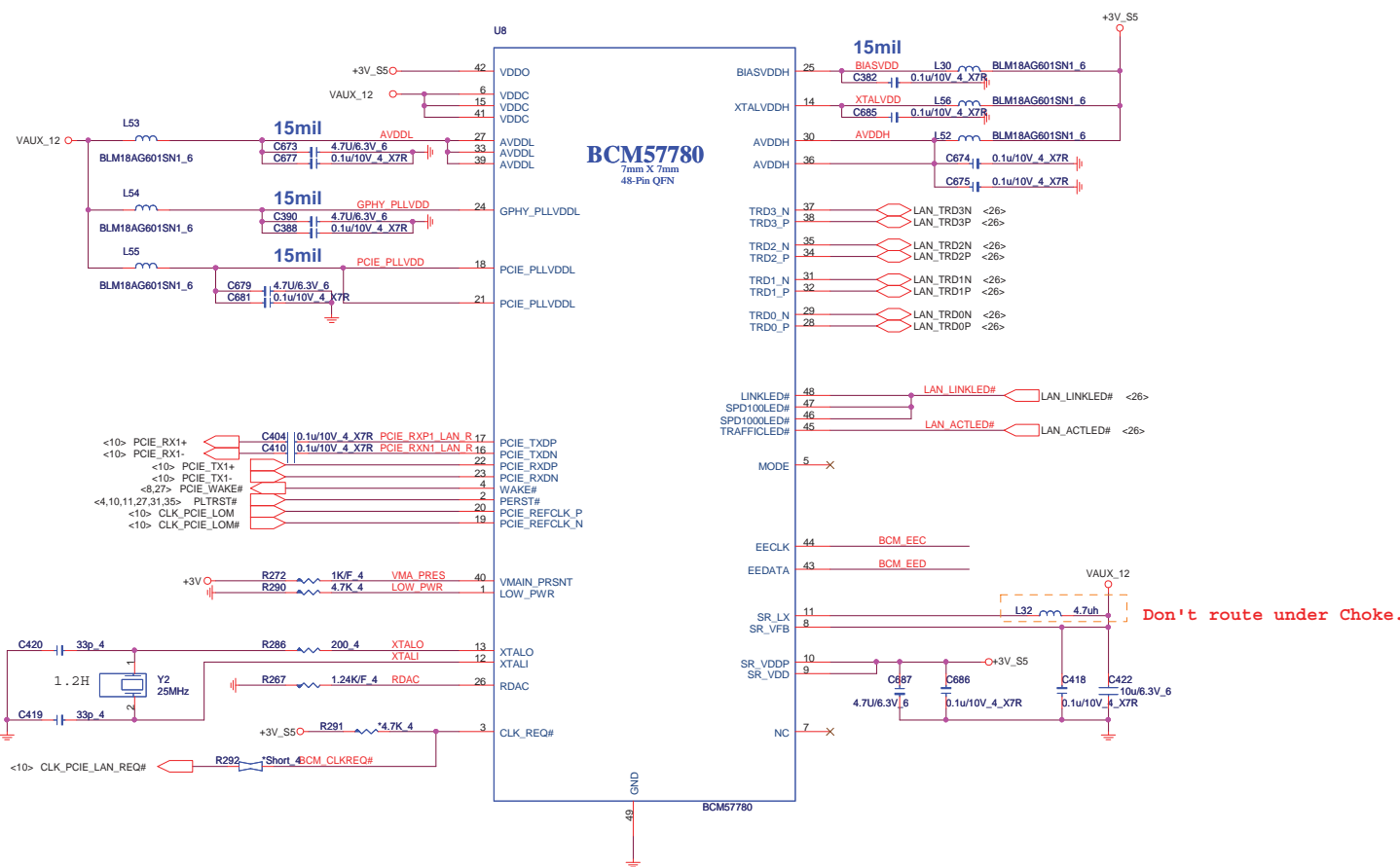
EMI



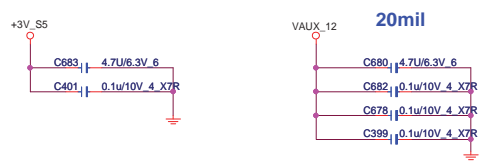
HDMI connector



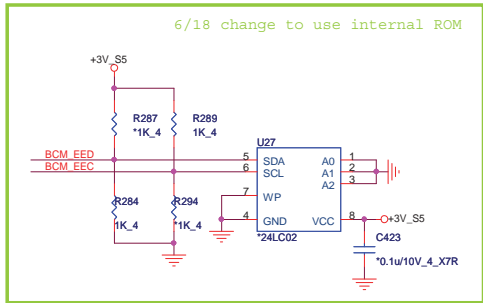
Giga-LAN BCM57780



LAN POWER



EEPROM



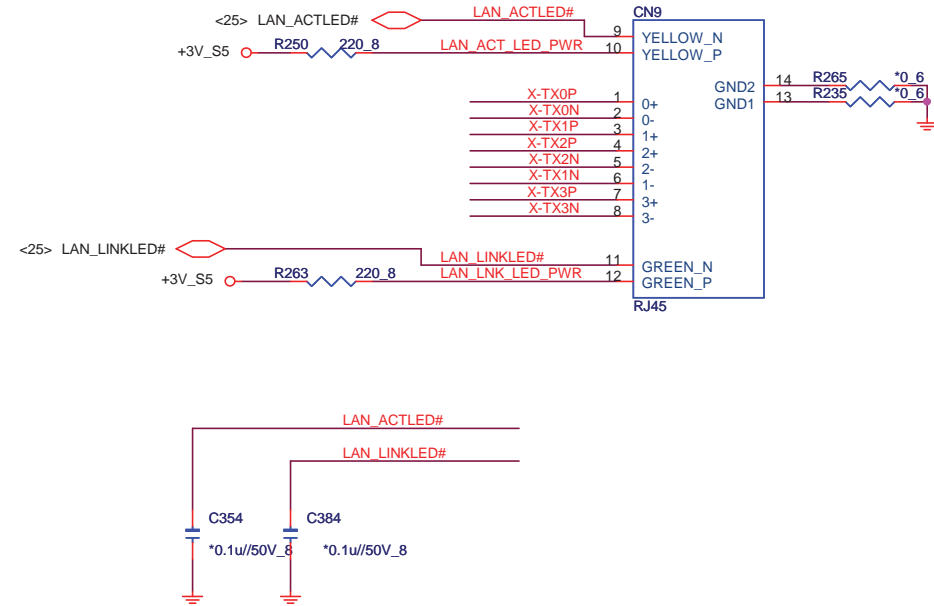
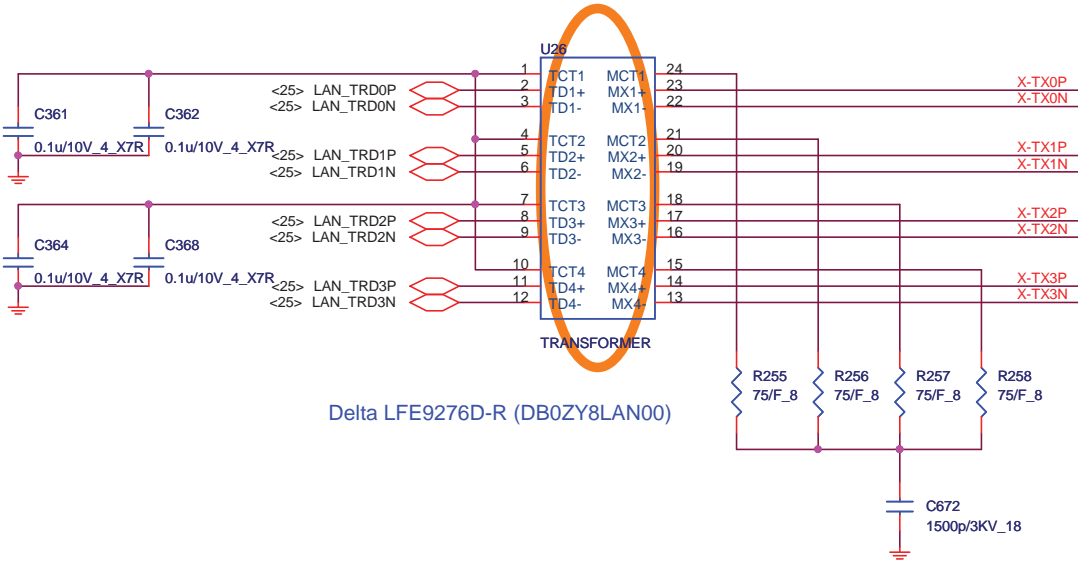
EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

A version Still mount the EEPROM

<http://hobi-elektronika.net>

TRANSFORMER



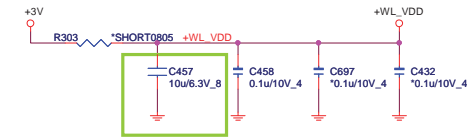
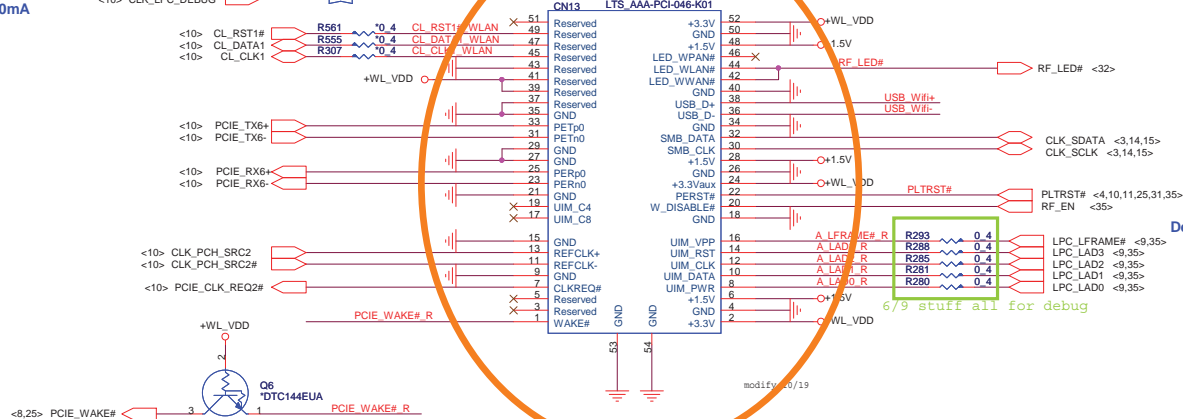
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux: 330mA
+1.5V: 500mA

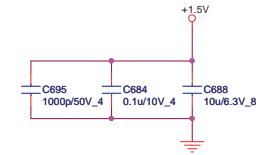
Debug

Check LED signal. (active high or low)

H=7.0mm
LTS AAA-PCI-046-K01



5/13 change to 6.3V



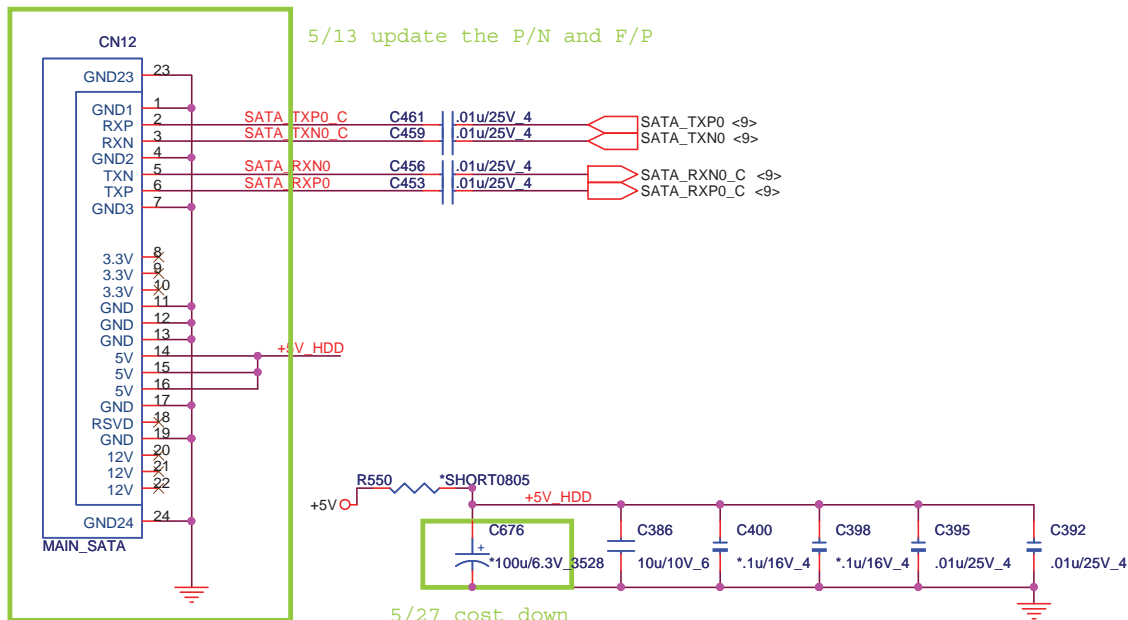
Debug

USB_Wifi+ R575 0.4
USB_Wifi- R576 0.4

6/9 stuff all for debug

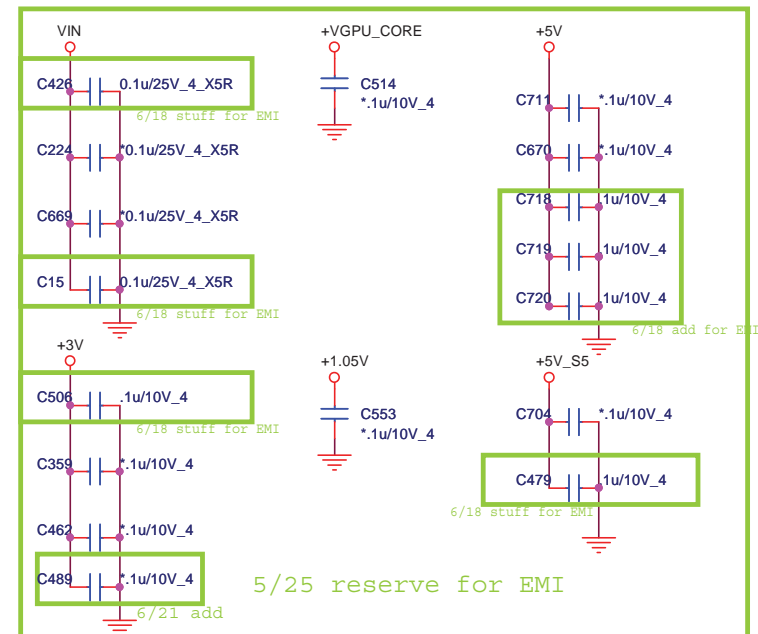
MAIN SATA HDD

5/13 update the P/N and F/P



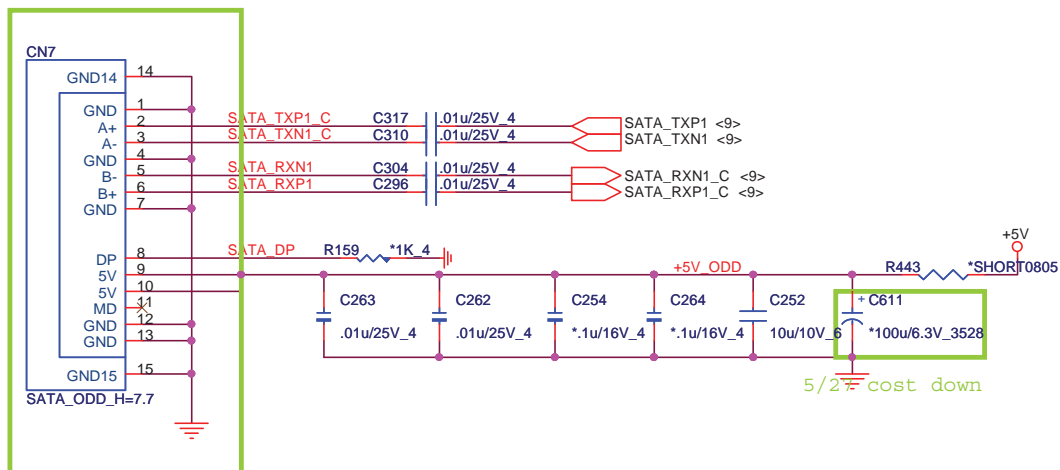
5/27 cost down

EE RETURN-PATH CAPACITORS



5/25 reserve for EMI

ODD (SATA)



5/27 cost down

5/26 change the footprint



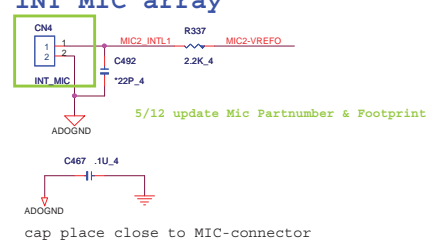
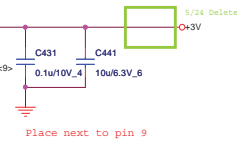
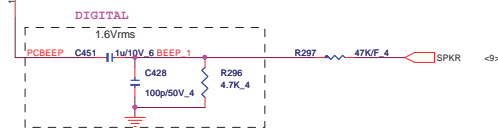
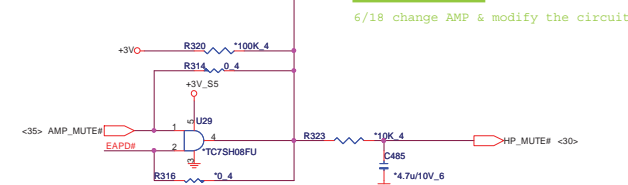
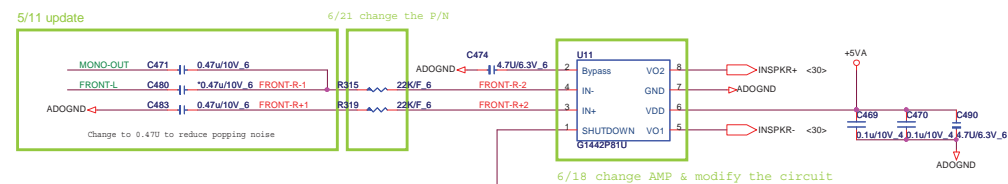
Quanta Computer Inc.

PROJECT : ZQ9

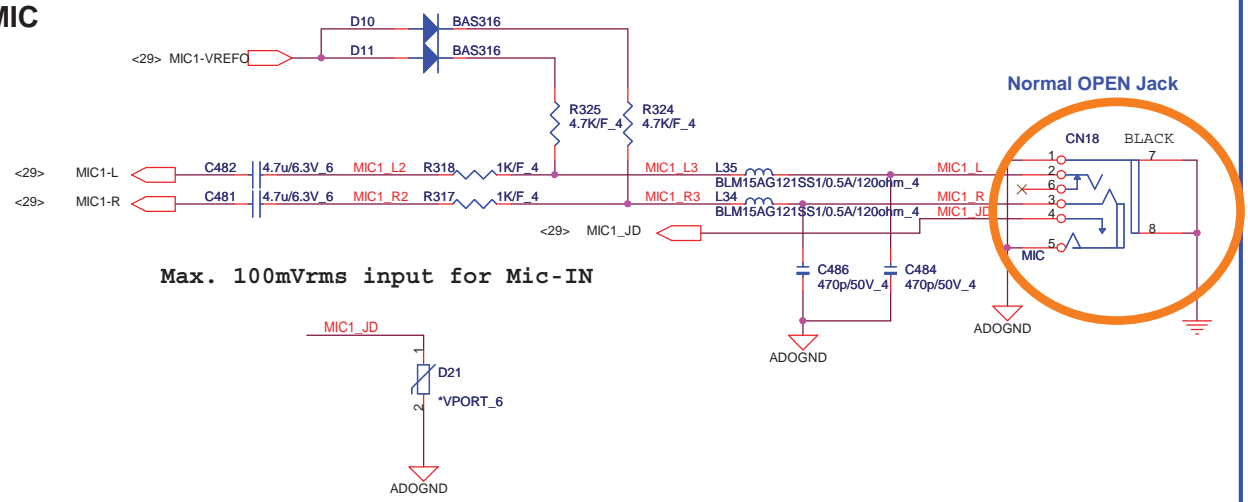
Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A

Date: Tuesday, June 22, 2010 Sheet 28 of 45

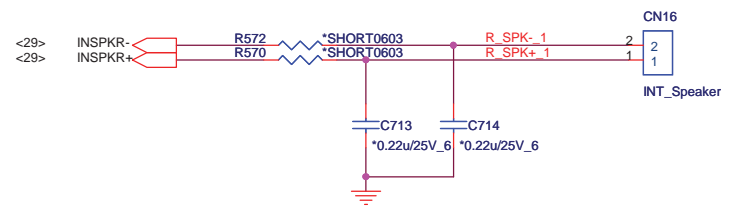
MUTE(AMP)



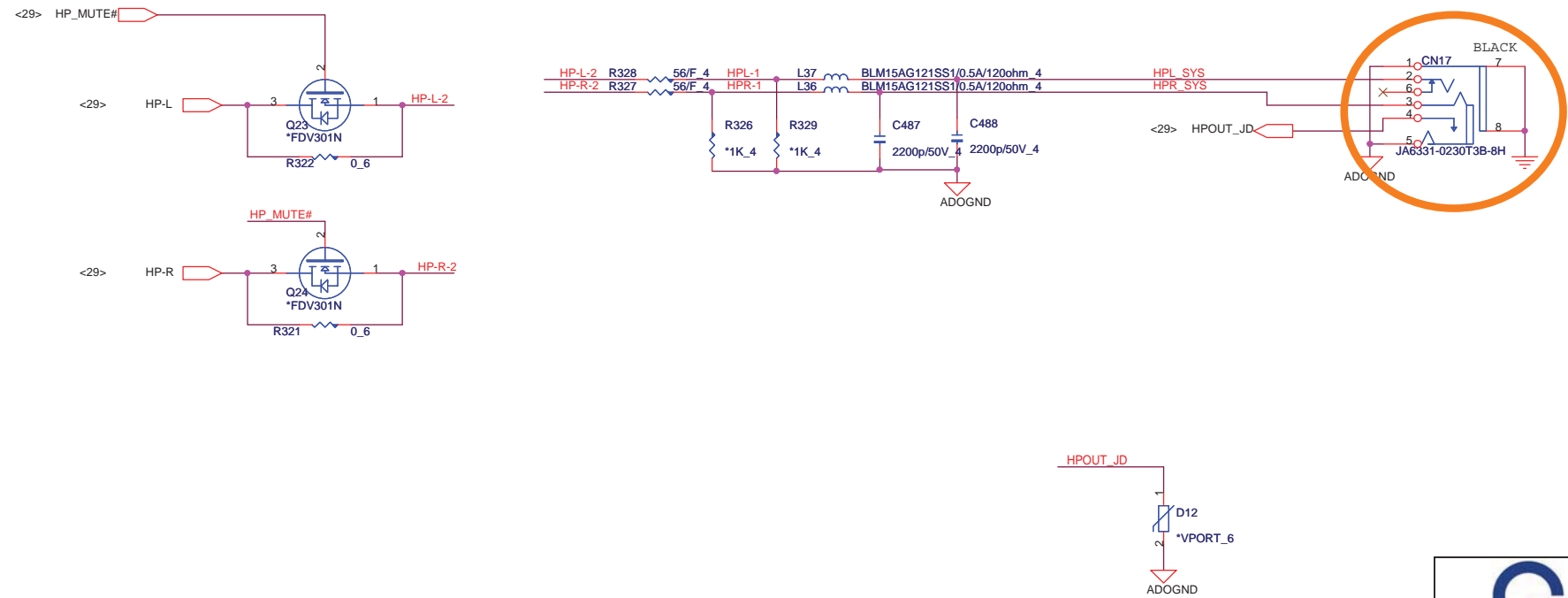
MIC




Internal Speaker



HP/SPDIF





Quanta Computer Inc.

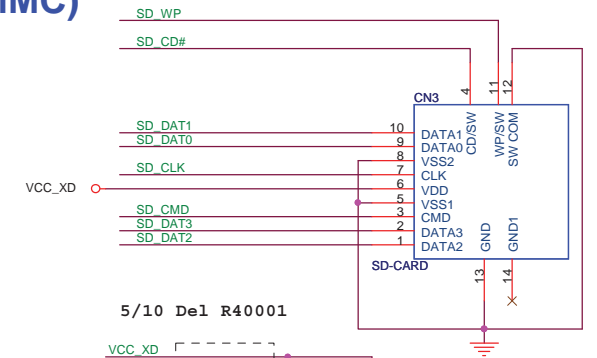
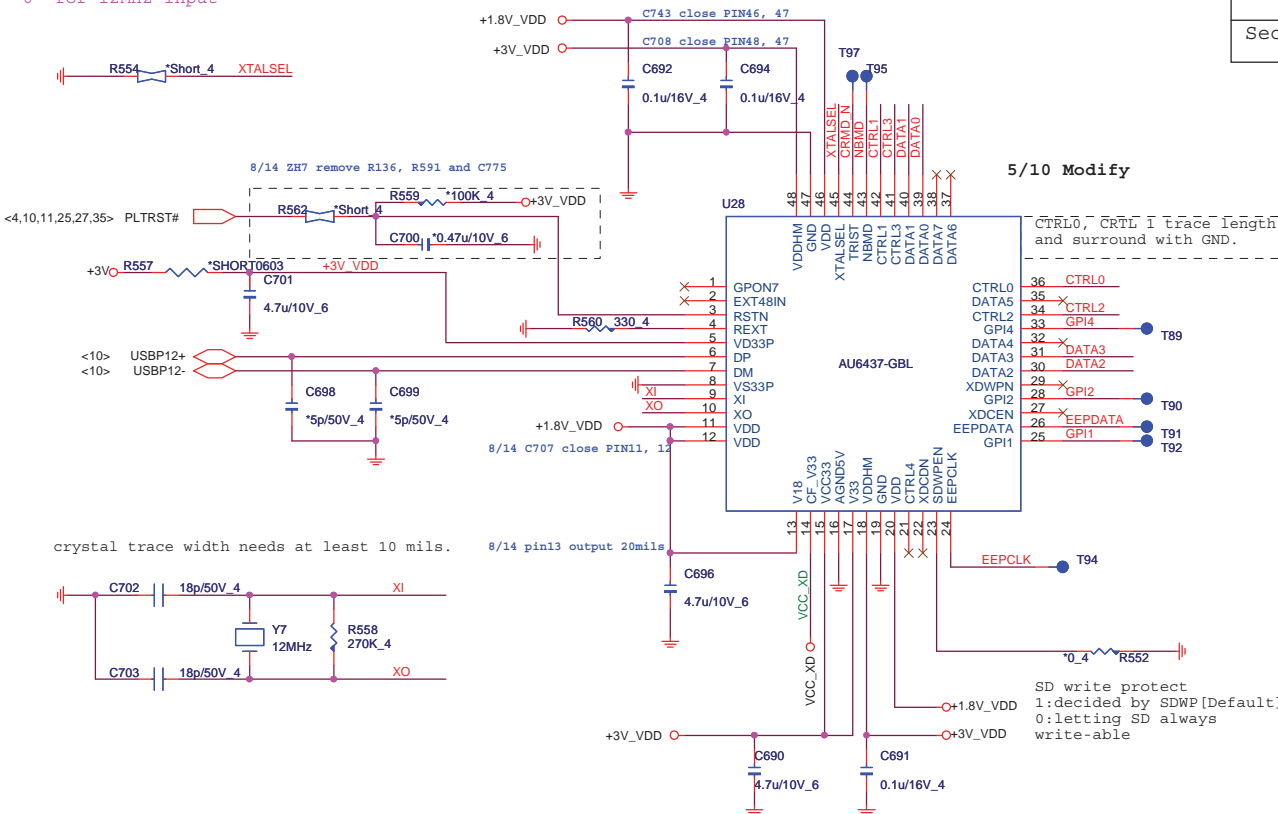
PROJECT : ZQ9

Size	Document Number	Rev
AMP /AUDIO JACK CONN		1A
Date:	Tuesday, June 22, 2010	Sheet 30 of 45

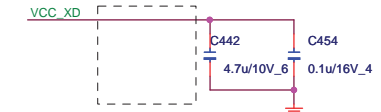
CARD READER Controller

2 IN 1 CARD READER (SD/MMC)

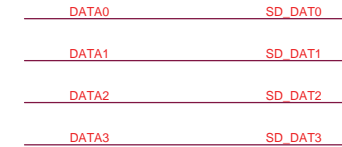
Clock input selection
'1' for 48MHz input [Default, Internal PU]
'0' for 12MHz input



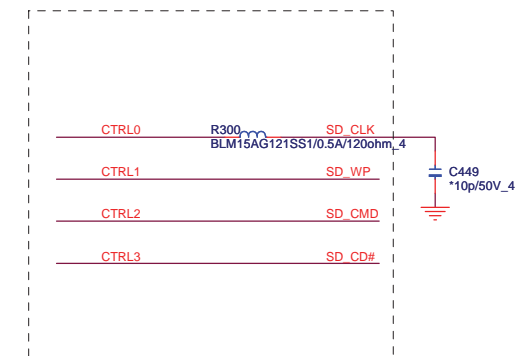
5/10 Del R40001



5/10 change Card Redaer conn
footpirt sdcard-sdsn09-08-xa-11p-smt



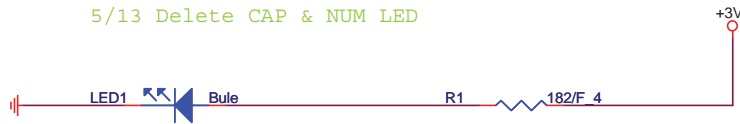
Close to connector



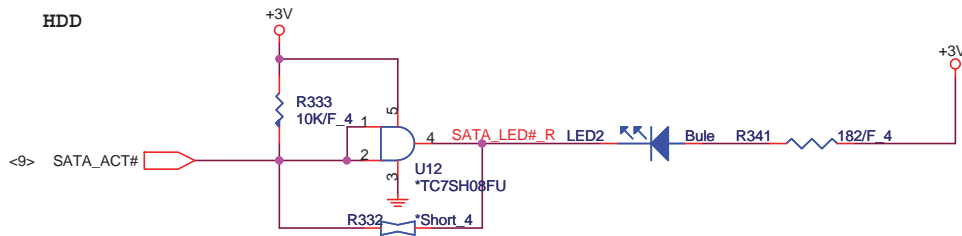
LED

5/13 Delete CAP & NUM LED

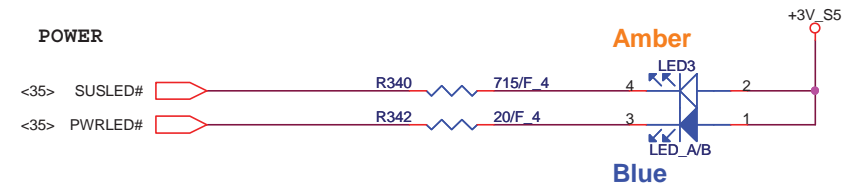
Power LED



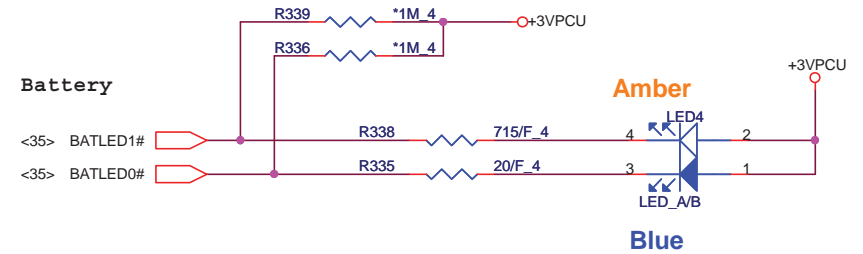
HDD



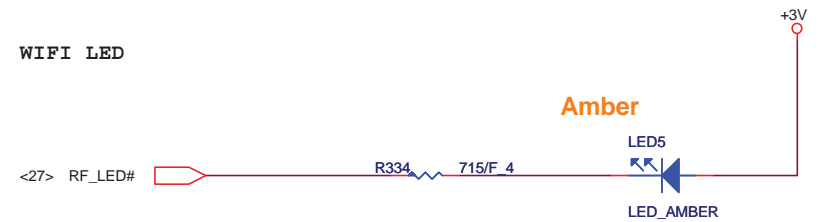
POWER



Battery



WIFI LED



Quanta Computer Inc.

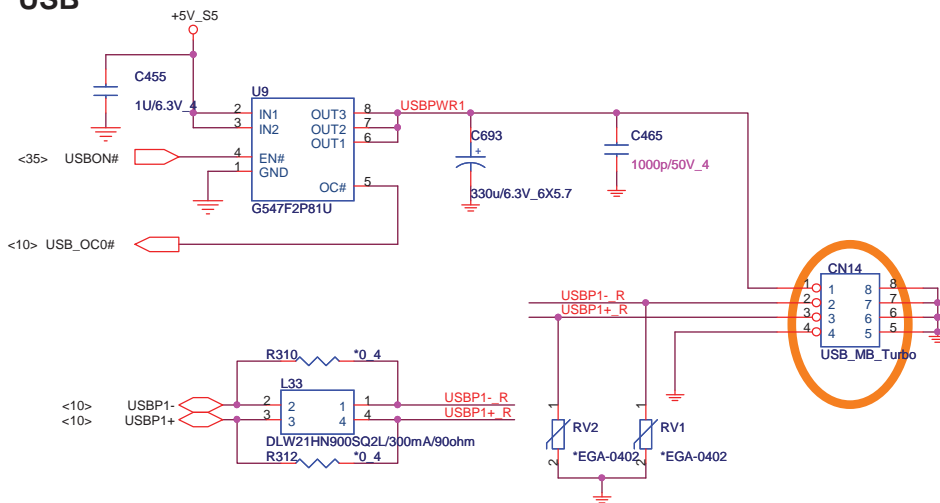
PROJECT : ZQ9

POWER/MMB/LAUNCH/LED

Size	Document Number	Rev 1A
------	-----------------	--------

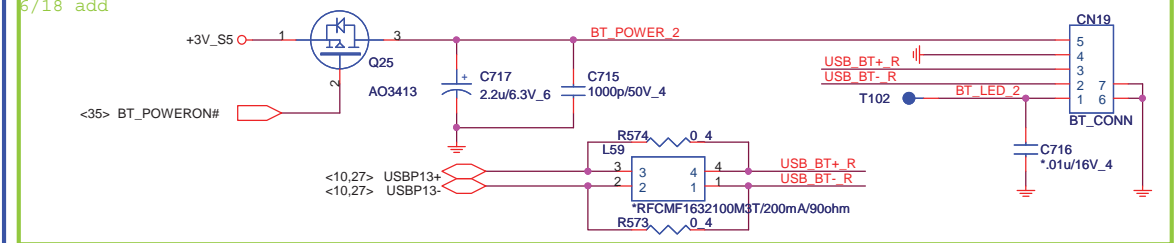
Date: Tuesday, June 22, 2010	Sheet 32 of 45
------------------------------	----------------

USB

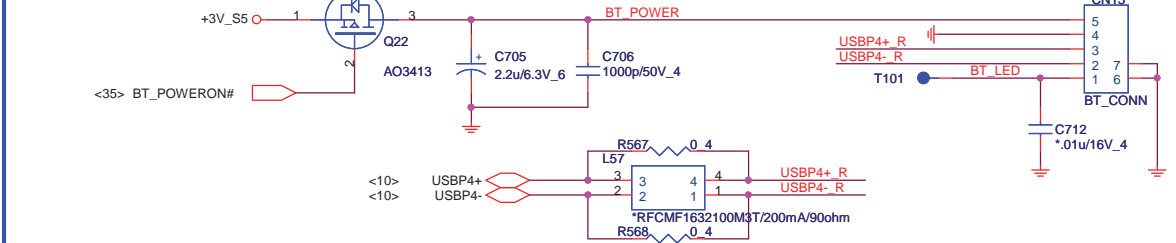


BLUETOOTH CONNECTOR for 2.0

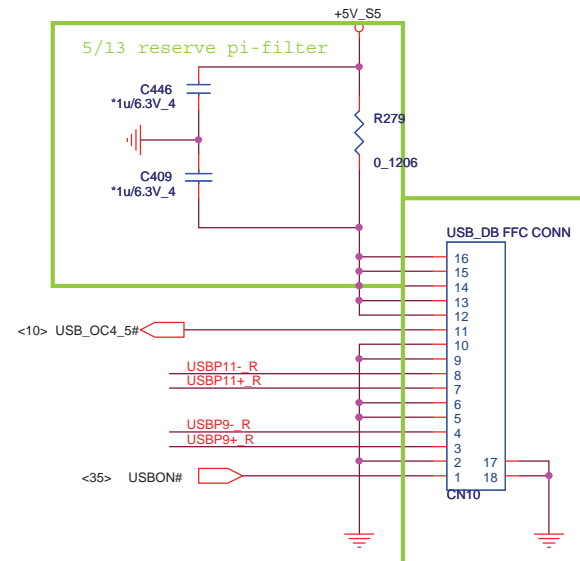
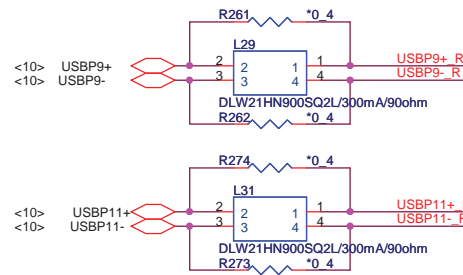
6/18 add



BLUETOOTH CONNECTOR for 3.0



USB/B



5/11 update the footprint

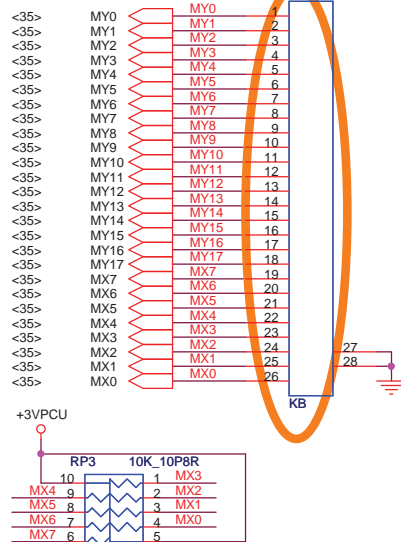


Quanta Computer Inc.

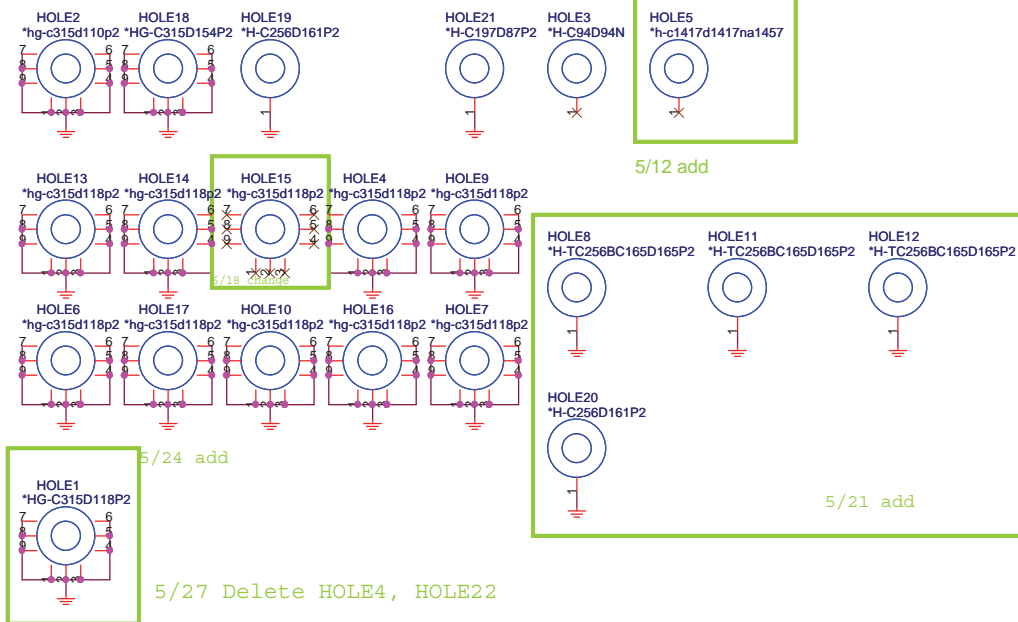
PROJECT : ZQ9

Size	Document Number	Rev
	USB/ BT	1A
Date:	Tuesday, June 22, 2010	Sheet 33 of 45

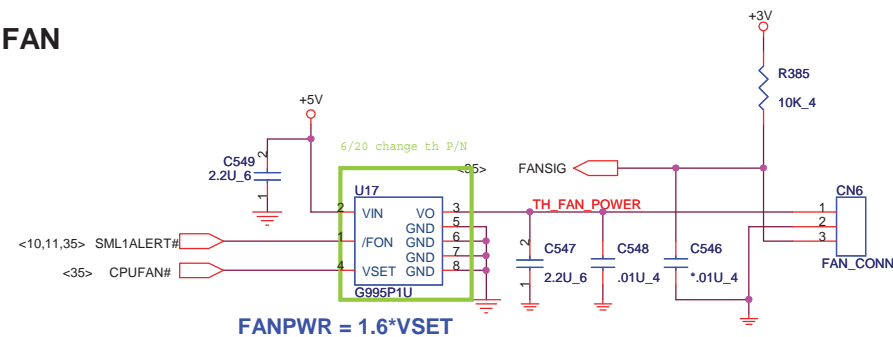
K/B



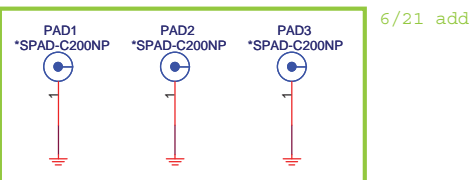
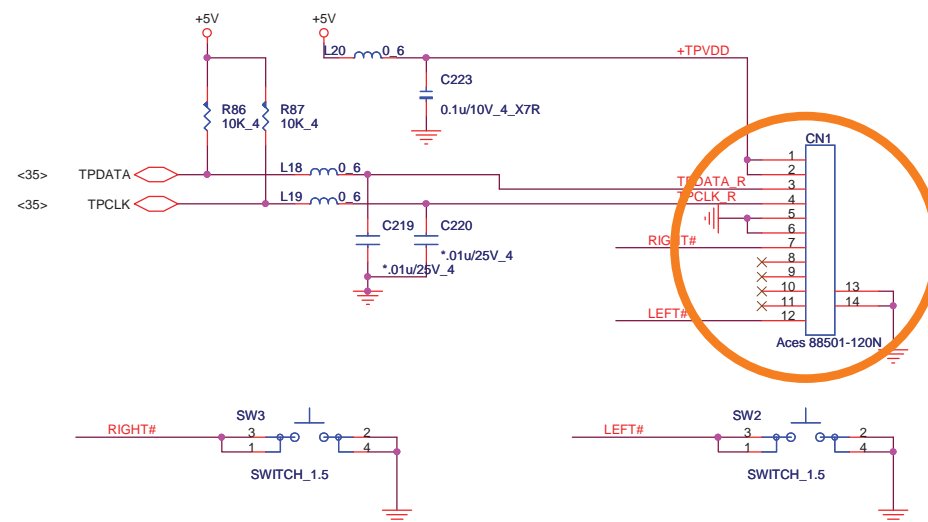
HOLE




CPU FAN

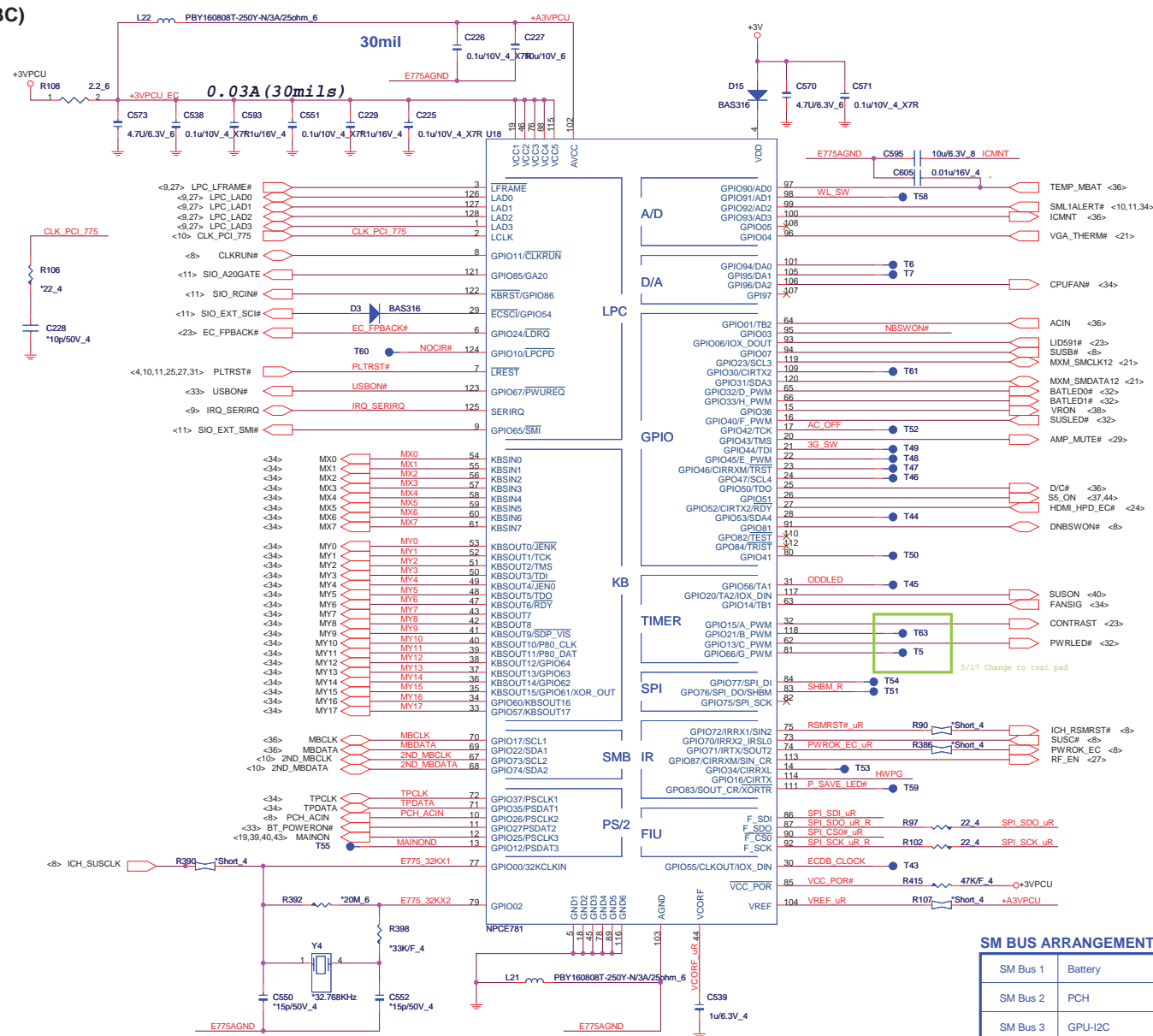


TOUCHPAD & Switch CONN

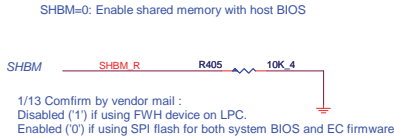


 <div> Quanta Computer Inc. PROJECT : ZQ9 </div>		Rev 1A
Size	Document Number	
KB/FAN/TP+FP		
Date:	Tuesday, June 22, 2010	Sheet 34 of 45

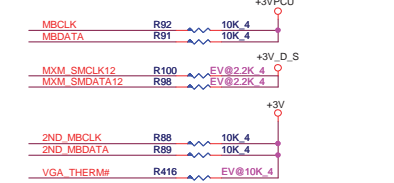
EC(KBC)



I/O ADDRESS SETTING(KBC)



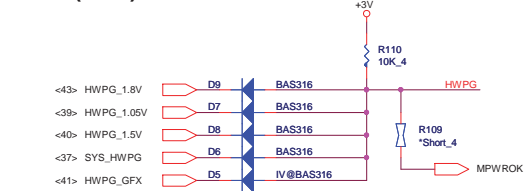
SM BUS PU(KBC)



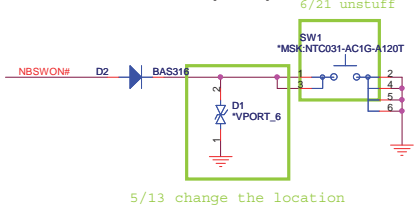
SPI FLASH(KBC)



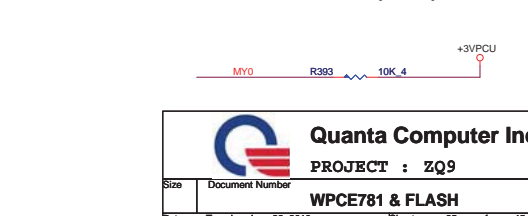
HWPG(KBC)



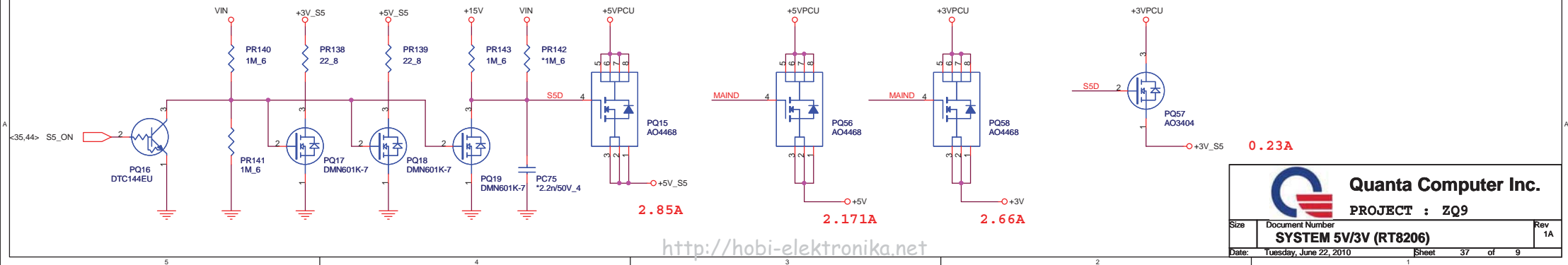
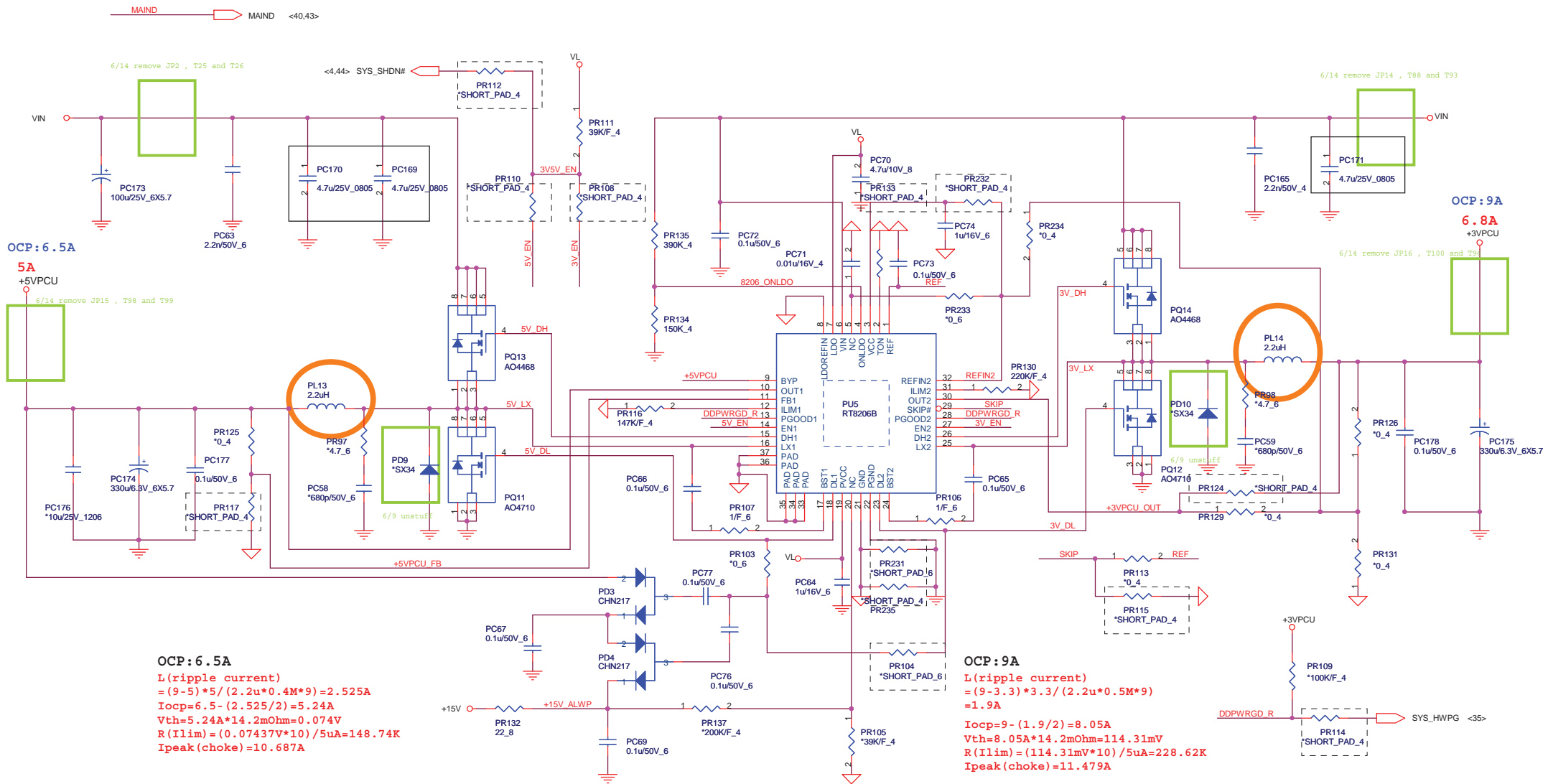
POWER-ON Switch(KBC)

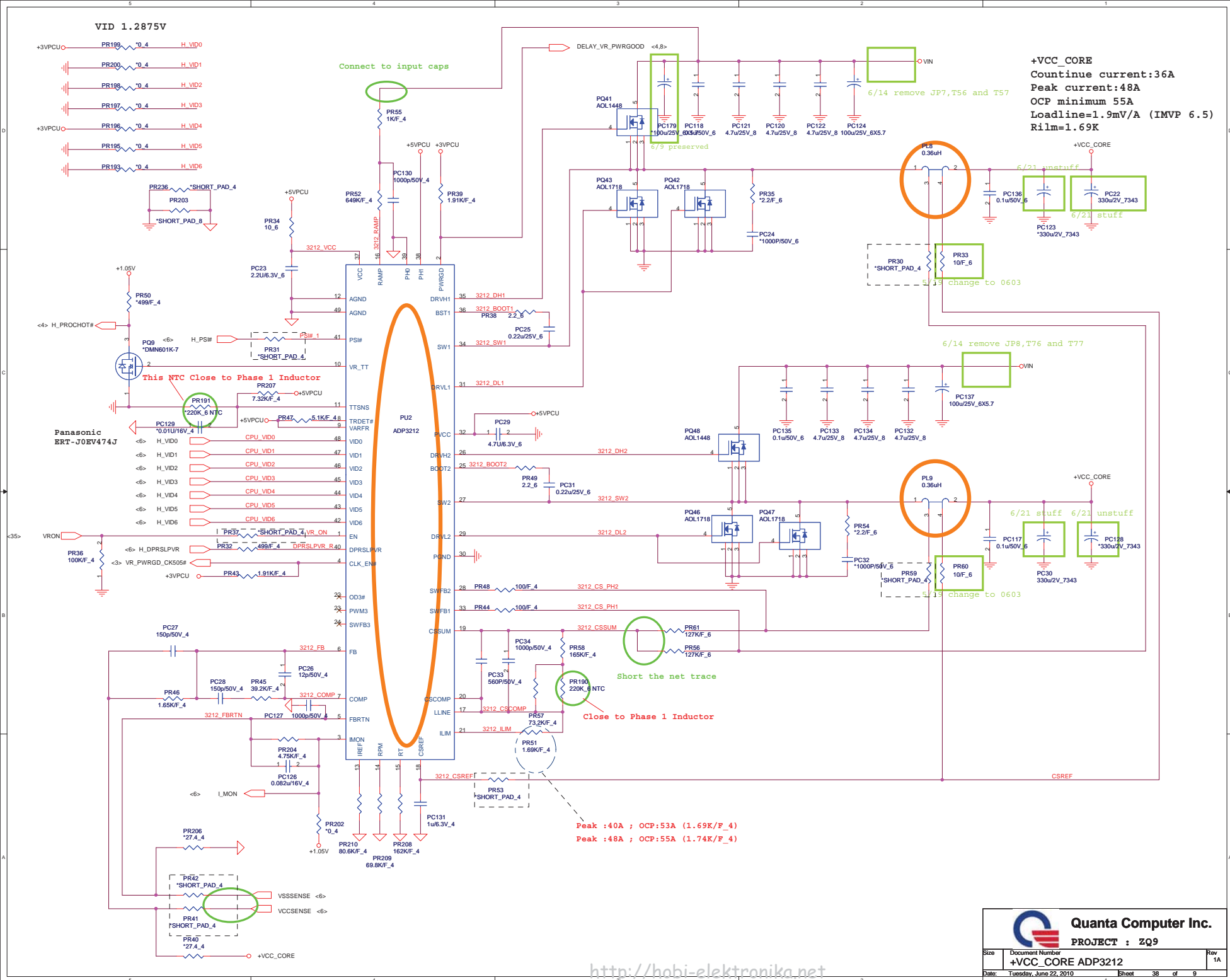


INTERNAL KEYBOARD STRIP SET(KBC)

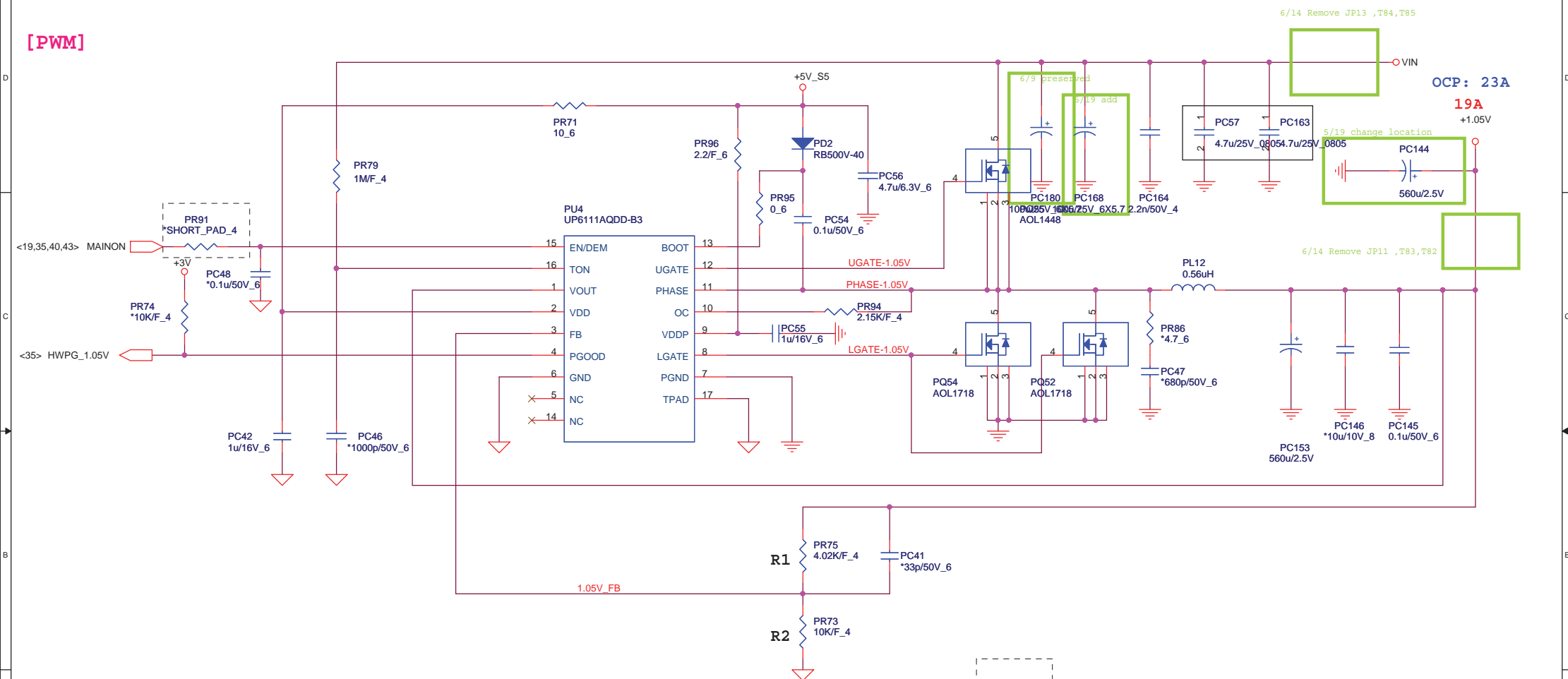


SM BUS ARRANGEMENT TABLE	
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A





[PWM]



$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

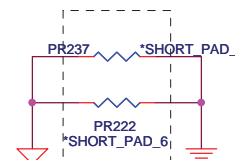
$$Frequency = 1 / (0.0036767) = 272K$$

A01718 $R_{dson} = 3 \sim 4.3m\Omega$

$$L(ripple\ current) = (19 - 1.05) \cdot 1.05 / (0.56u \cdot 272k \cdot 19) \sim 6.512A$$

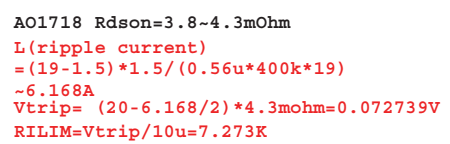
$$RILIM = 2.15m\Omega \cdot 23 - 3.256 / 20uA = 2.122K\Omega$$

$$I(choke)_{peak} = 29.512A$$

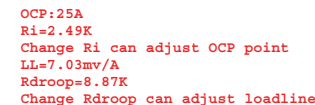


Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	+VTT (UP6111A)	1A
Date:	Tuesday, June 22, 2010	Sheet 39 of 9



	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF





<http://hobi-elektronika.net>